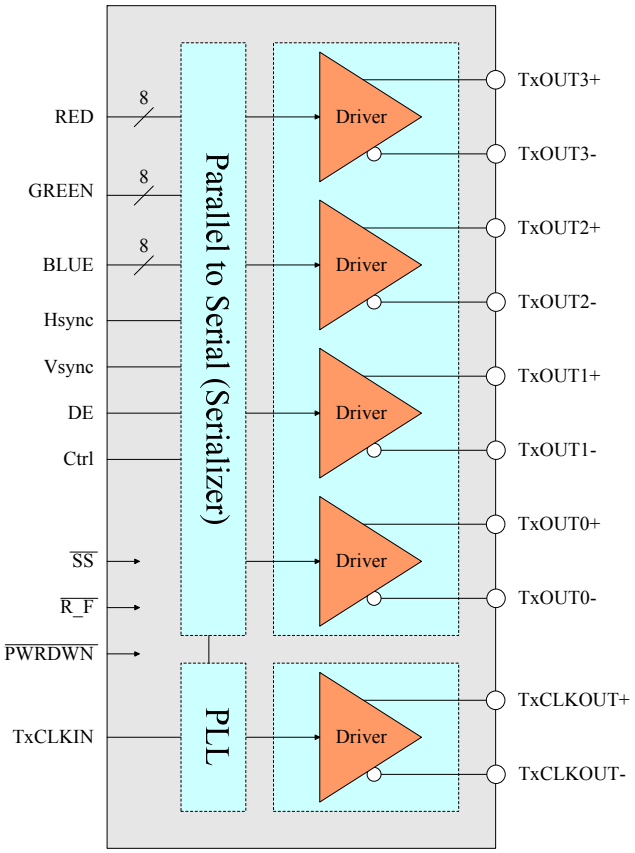
Introduction

The CL12463C transmitter converts parallel 28bits (24bits of RGB data and 4bits of HSYNC, VSYNC, DE and Control) of LVCMOS parallel data into serial four LVDS data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. The CL12463C transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin. At a transmit clock frequency of 85MHz, 24bits of RGB data and 4bits of LCD timing and control data (HSYNC, VSYNC, DE, Control1) are transmitted at a rate of 595Mbps per LVDS data channel. The CL12463C transmitter is an ideal means to solve EMI and cable size problems associated with wide, high-speed CMOS interfaces.

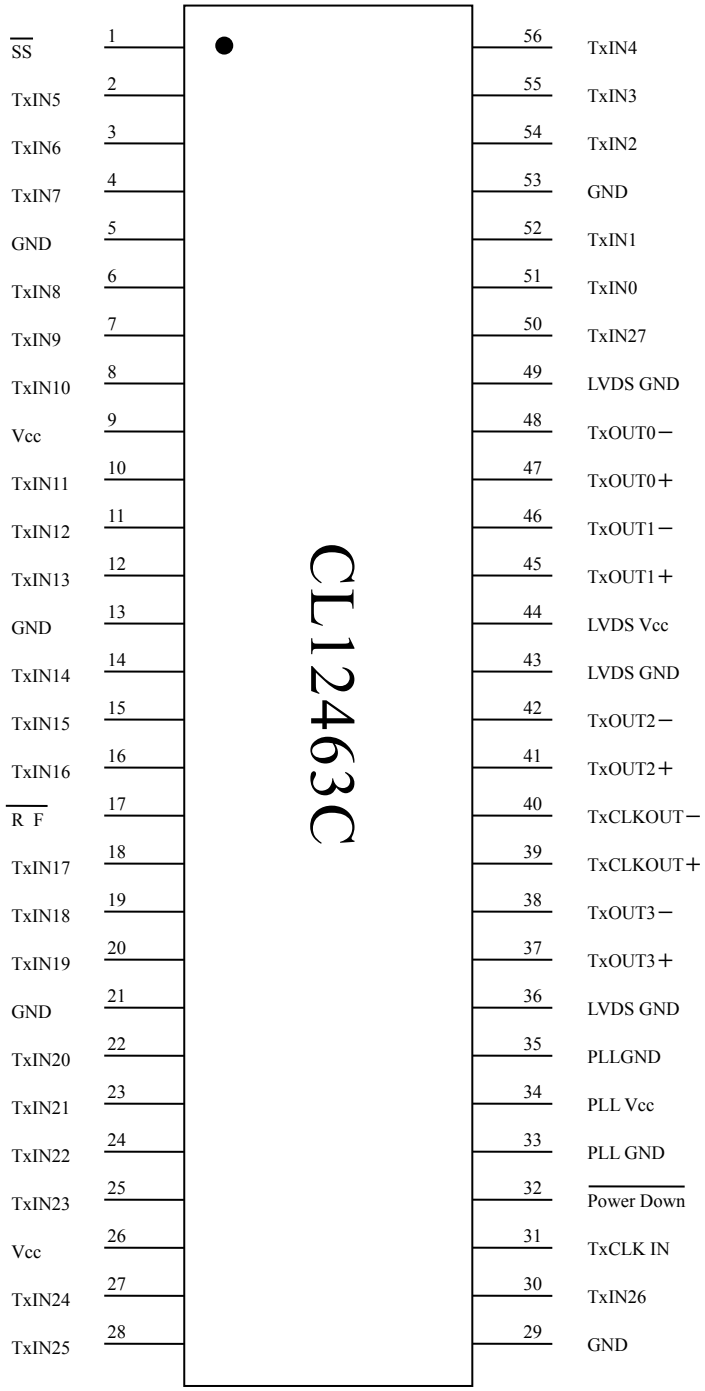
Feature

- Input Clock: 20MHz to 85MHz shift clock support
- Output Clock: 20MHz~85MHz Output Data Rate: 140Mbps~595Mbps
- Low power single 3.3V
- Clock edge programmable
- Supports VGA, SVGA, XGA, SXGA, SXGA+
- Narrow bus reduces cable size
- PLL requires no external components
- Power down mode
- Low Profile 56 Lead TSSOP Package
- 345mV swing LVDS devices for low EMI
- Supports 200mV Differential Amplitude Outputs
- Pin Compatible with DS90C383/385, THC63LVDM83R

Block Diagram



Pin Configuration



Pin Description

Pin Name	No of Pin	I/O	Pin Description
TxIN	28	IN	LVCMOS Data Inputs
TxOUT+	4	OUT	Positive LVDS Differential Data Outputs
TxOUT-	4	OUT	Negative LVDS Differential Data Outputs
TxCLKIN	1	IN	LVCMOS Level Clock Input
TxCLKOUT+	1	OUT	Positive LVDS Differential Clock Output
TxCLKOUT-	1	OUT	Negative LVDS Differential Clock Output
$\overline{\text{Power Down}}$	1	IN	H: Normal Operation L: Power Down (all Outputs are Hi-Z)
$\overline{\text{R\_F}}$	1	IN	Programmable Strobe Select H: Rising Edge, L: Falling Edge
$\overline{\text{SS}}$	1	IN	Programmable Differential Amplitude Voltage Select H: 345mV, L: 200mV
Vcc / GND	3/5	IN	Power Supply/Ground Pins for LVCMOS Inputs
PLL Vcc / PLL GND	1/2	IN	Power Supply/Ground Pins for PLL
LVDS Vcc / LVDS GND	2/4	IN	Power Supply/Ground Pins for LVDS Outputs

Absolute Maximum Ratings

Supply Voltages	-0.3V to +4V
CMOS/TTL Input Voltage	-0.3V to (Vcc+0.3V)
LVDS Driver Output Voltage	-0.3V to (Vcc+0.3V)
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150 ℃
Storage Temperature	-65 ℃ to +150 ℃
Lead Temperature (Soldering, 4sec)	+260 ℃
Maximum Power Dissipation Capacity (25℃)	1.4 W

Electrical Characteristics

1. LVCMOS DC Specification — Vcc=3.0V to 3.6V Ta=-10℃ to 70℃

Symbol	Parameter	Conditions	min	typ	max	unit
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	
I_{PD}	Pull Down Current	$\overline{R\_F}$ pin, $V_{IH}=V_{CC}$			100	μA
I_{IN}	Input Current	$V_{IN}=V_{CC}$,GND,2.5V or 0.4V			100	

2. LVDS DC Specification — Vcc=3.0V to 3.6V Ta=-10℃ to 70℃

Symbol	Parameter	Conditions		min	typ	max	unit
V_{OD}	Differential Output Voltage	R_L=100 Ohm	SS=V_{CC}	250	345	450	mV
			SS=0V	100	200	300	
ΔV_{OD}	Change in V_{OD} between Complimentary Output states	R_L=100 Ohm				35	mV
V_{CM}	Common Mode Voltage			1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between Complimentary Output states					35	mV
I_{OS}	Output Short Circuit Current	V_{OUT}=0V,R_L=100 Ohm				-5	mA
I_{OZ}	Output Tri-State Current	$\overline{\text{Power Down}}$=0V,$V_{OUT}$=0V or V_{CC}				±10	μA

3. Transmitter Supply Current — Vcc=3.0V to 3.6V Ta=-10℃ to 70℃

Symbol	Parameter	Conditions		min	typ	max	unit
ICCTW	Transmitter Supply Current	R_L=100Ohm C_L=5pF Worst Case Pattern	f=65MHz		51	61	mA
			f=85MHz		55	64	
ICCTG		R_L=100Ohm C_L=5pF 16Gray Scale Pattern	f=65MHz		40	54	
			f=85MHz		43	57	
ICCTZ		$\overline{\text{Power Down}}$=Low				10	μA

4. Switching Characteristics Vcc=3.0V to 3.6V Ta=-10℃ to 70℃

Symbol	Parameter	min	typ	max	unit
TCIT	TxCLK IN Transition Time			5	ns
TCIP	TxCLK IN Period	7.41	T	50	
TCIH	TxCLK IN High Time	0.35T	0.5T	0.65T	
TCIL	TxCLK IN Low Time	0.35T	0.5T	0.65T	
LLHT	LVDS Low to High Transition Time		0.6	1.5	
LHLT	LVDS High to Low Transition Time		0.6	1.5	
TCCS	TxOUT Channel to Channel Skew		250		ps
$TPP_{OS}0$	Transmitter Output Pulse Position for Bit 0,f=85MHz	-0.2	0	+0.2	ns
$TPP_{OS}1$	Transmitter Output Pulse Position for Bit 1,f=85MHz	T/7-0.2	T/7	T/7+0.2	
$TPP_{OS}2$	Transmitter Output Pulse Position for Bit 2,f=85MHz	2T/7-0.2	2T/7	2T/7+0.2	
$TPP_{OS}3$	Transmitter Output Pulse Position for Bit 3,f=85MHz	3T/7-0.2	3T/7	3T/7+0.2	
$TPP_{OS}4$	Transmitter Output Pulse Position for Bit 4,f=85MHz	4T/7-0.2	4T/7	4T/7+0.2	
$TPP_{OS}5$	Transmitter Output Pulse Position for Bit 5,f=85MHz	5T/7-0.2	5T/7	5T/7+0.2	
$TPP_{OS}6$	Transmitter Output Pulse Position for Bit 6,f=85MHz	6T/7-0.2	6T/7	6T/7+0.2	
TSTC	TxIN Setup to TxCLK IN	2.5			ns
THTC	TxIN Hold to TxCLK IN	0			
TCCD	TxCLK IN to TxCLK OUT Delay	3.0	3.7	5.5	
TPLLS	Transmitter Phase Lock Loop Set			10	ms
TPDD	Transmitter Power Down Delay			100	ns

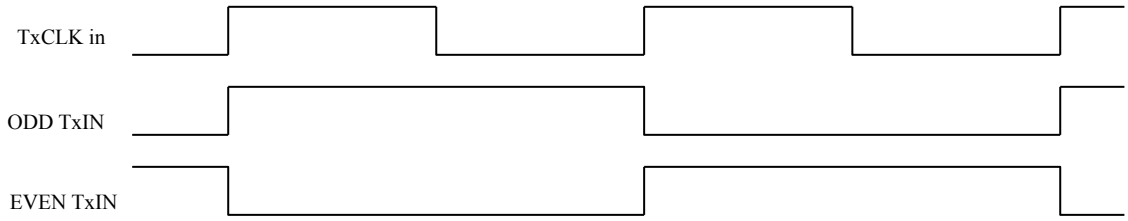


Fig.1 Worst Case Test Pattern

PIN Name	Signal	Signal Pattern	Signal Frequency
TxCLK IN	DOT CLK		f
TxIN0	R0		f/16
TxIN1	R1		f/8
TxIN2	R2		f/4
TxIN3	R3		f/2
TxIN4	R4		Steady State, Low
TxIN6	R5		Steady State, Low
TxIN27	R6		Steady State, Low
TxIN5	R7		Steady State, Low
TxIN7	G0		f/16
TxIN8	G1		f/8
TxIN9	G2		f/4
TxIN12	G3		f/2
TxIN13	G4		Steady State, Low
TxIN14	G4		Steady State, Low
TxIN10	G6		Steady State, Low
TxIN11	G7		Steady State, Low
TxIN15	B0		f/16
TxIN18	B1		f/8
TxIN19	B2		f/4
TxIN20	B3		f/2
TxIN21	B4		Steady State, Low
TxIN22	B5		Steady State, Low
TxIN16	B6		Steady State, Low
TxIN17	B7		Steady State, Low
TxIN23	CNTL		Steady State, Low
TxIN24	HSYNC		Steady State, High
TxIN25	VSYNC		Steady State, High
TxIN26	DE		Steady State, High

Fig.2 16-Grayscale Test Pattern

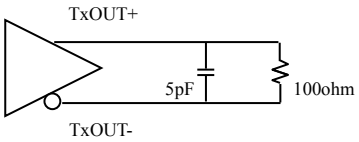


Fig.3: LVDS Output Load

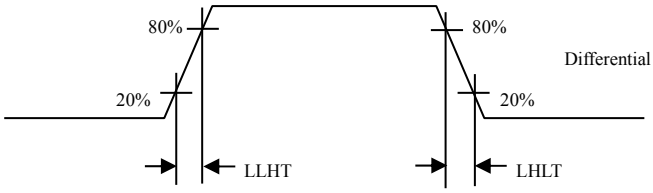


Fig.4: LVDS Transition Times

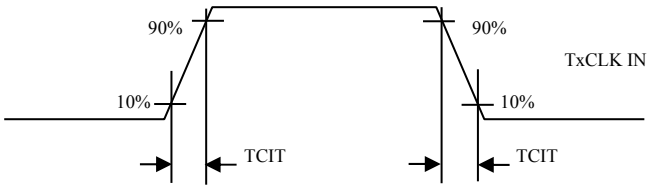


Fig.5: Input Clock Transition Times

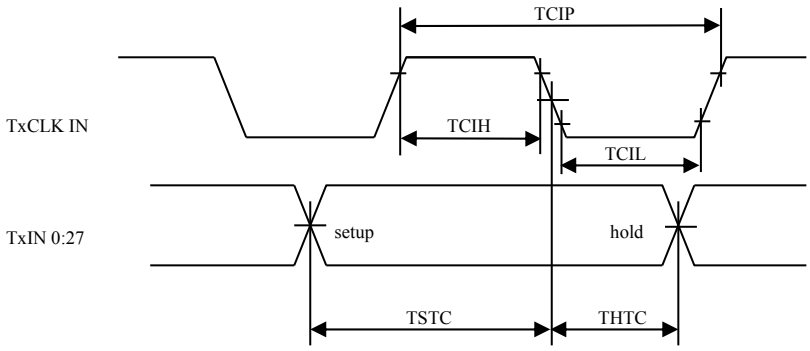


Fig.6: Transmitter Setup/hold and Low/High Times (Falling Edge Strobe)

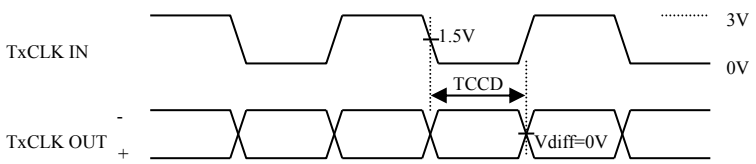


Fig.7: Transmitter Clock in to Clock out Delay (Falling Edge Strobe)

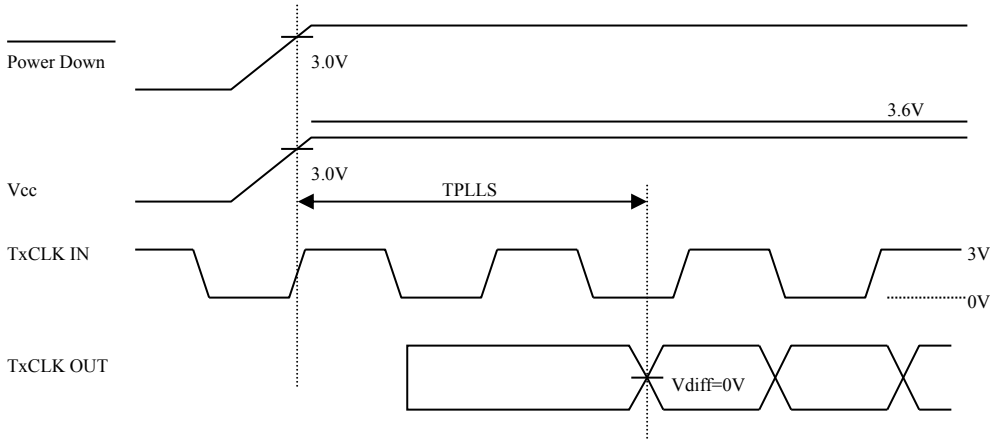


Fig.8: Transmitter Phase Lock Loop Setup Time

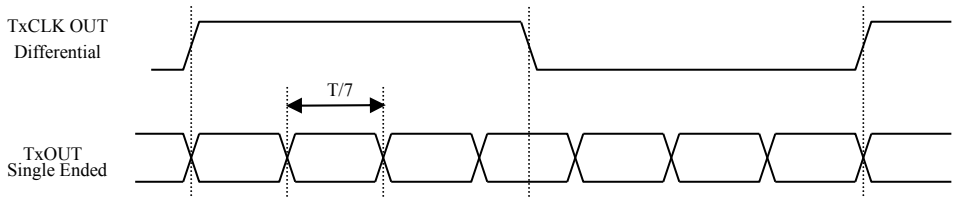


Fig.9: Seven Bits of LVDS in Once Cycle

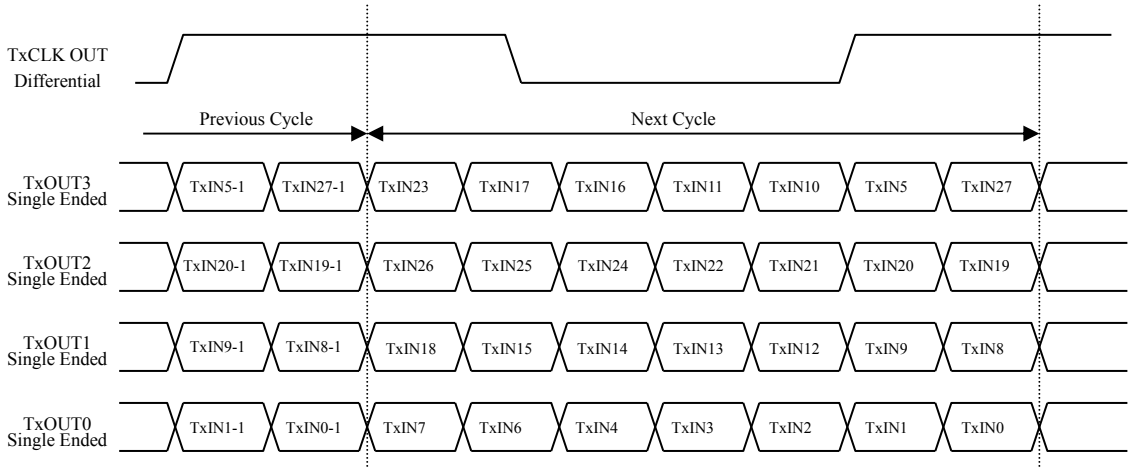


Fig.10: Parallel LVCMOS Data Inputs Mapped to LVDS Outputs

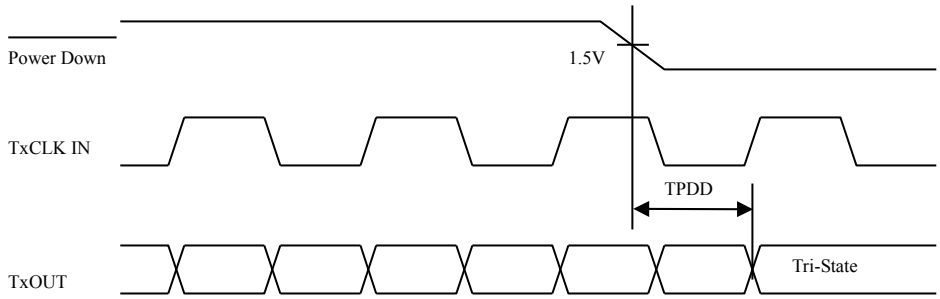


Fig.11: Transmitter Power Down Delay

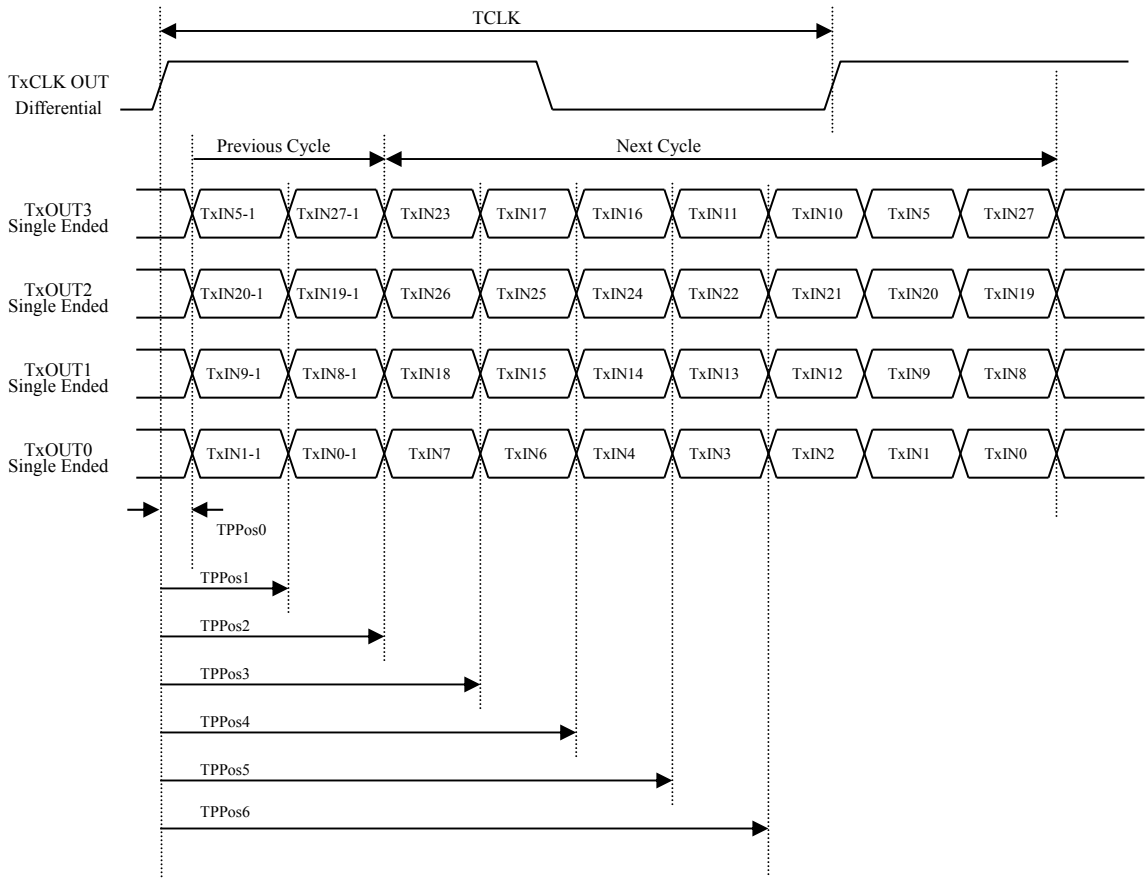
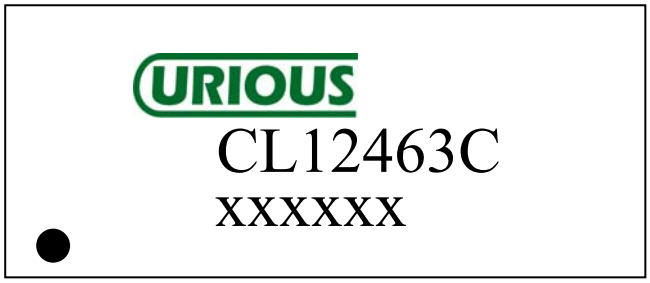


Fig.12: Transmitter LVDS Output Pulse Position Measurement


CL12463C
xxxxxx

Modification History

Version	Date	Contents
1.00	2010 / 1 / 12	1) Block Diagram changed
0.30	2007 / 7 / 18	1) Output Clock frequency & Data rate added
0.20	2006 / 5 / 23	1) From CL12463A to CL12463C changed 2) SS Mode (200mV Amplitude) added 3) Package LOGO changed 4) Supply Current value changed 5) Maximum Dot Clock Frequency changed 6) Transition Time Changed 7) TxCLKIN Cycle Time Changed
0.10	2005 / 5 / 10	Fig.2 Modified from 16-Gray to 1024-Gray
0.00	2003 / 5 / 15	First Version