Introduction

The CL12472IP270 receiver is designed to support dual pixel data transmission between Host and Flat Panel Display up to UXGA resolution. The receiver converts serial 8-LVDS data streams back into parallel 48bits (Dual Pixel 24-bit color) of LVCMOS data. Control signals (HSYNC, VSYNC, DE) are sent during blanking intervals. The CL12472IP270 receiver is an ideal means to solve EMI and cable size problems associated with wide, high-speed CMOS interfaces.

Feature

- 20MHz to 270MHz shift clock support
- Low power single 3.3V (Option: 2.8V) (Option: 1.0 / 1.2 / 1.8V Logic/Level Shifter)
- Clock edge programmable
- Supports VGA, SVGA, XGA, SXGA, UXGA
- Supports Dual Link and Single Link
- Supports RGB 18 / 24
- Narrow bus reduces cable size
- PLL requires no external components
- Power down mode
- Supports Fail-Safe function to all input channels

Block Diagram