

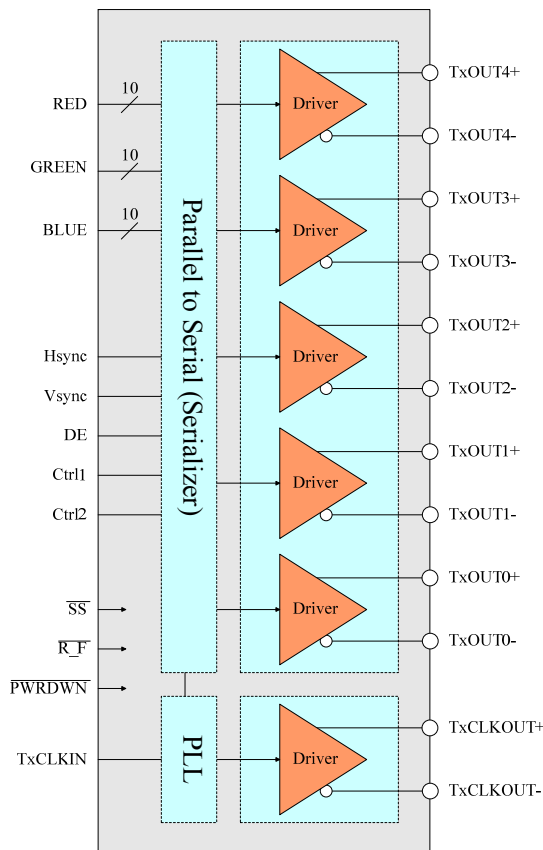
Introduction

The CL12481D transmitter converts parallel 35bits (30bits of RGB data and 5bits of HSYNC, VSYNC, DE and Control1, Control2) of LVCMOS data into serial 5-LVDS data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a sixth LVDS link. The CL12481D transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin. At a transmit clock frequency of 85MHz, 30bits of RGB data and 5bits of LCD timing and control data (HSYNC, VSYNC, DE, Control1, Control2) are transmitted at a rate of 595Mbps per LVDS data channel. The CL12481D transmitter is an ideal means to solve EMI and cable size problems associated with wide, high-speed LVCMOS interfaces.

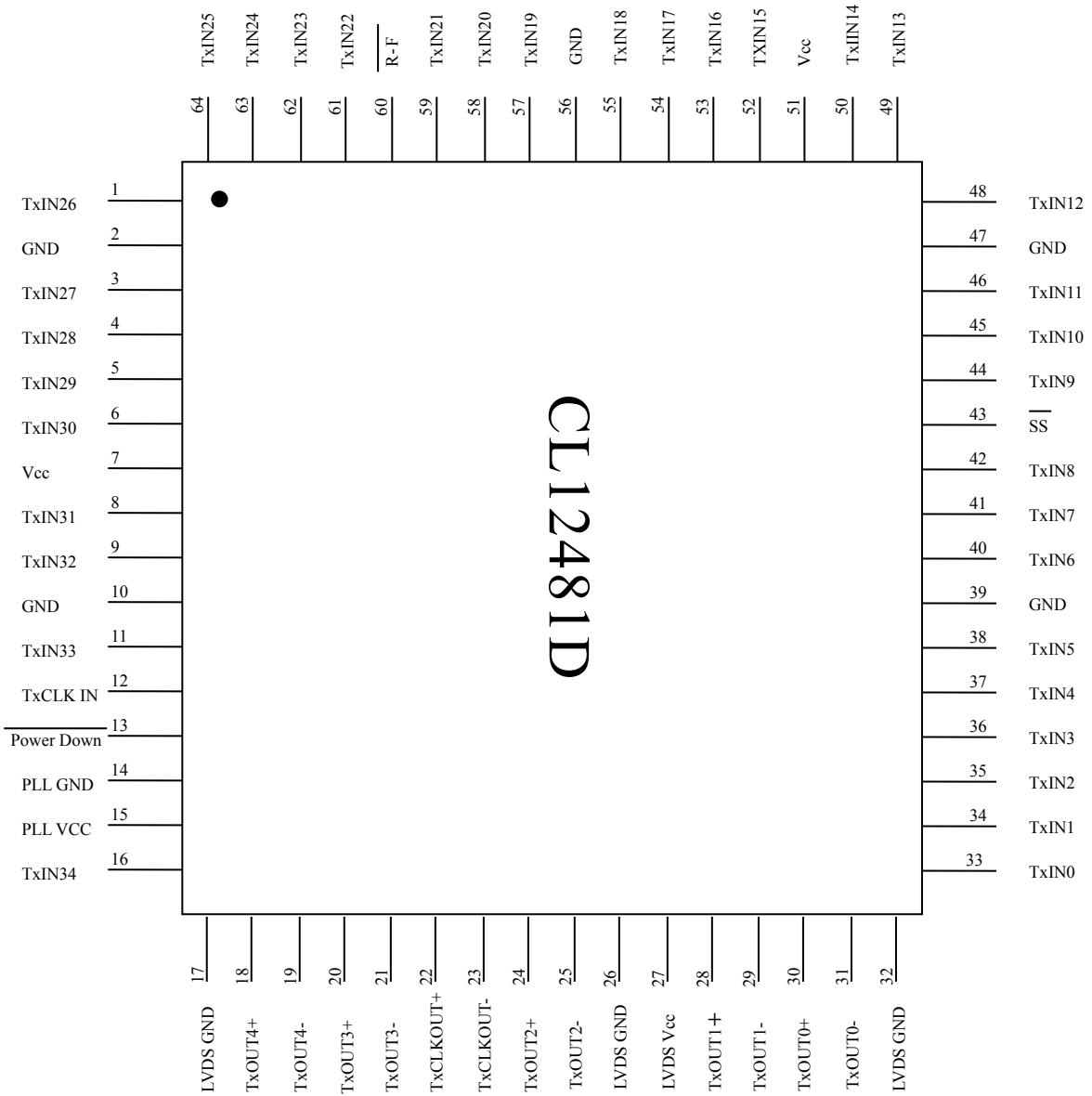
Feature

- Input Clock: 20MHz to 85MHz shift clock support
- Output Clock: 20MHz~85MHz Output Data Rate: 140Mbps~595Mbps
- Low power single 3.3V
- Clock edge programmable
- Supports VGA, SVGA, XGA, SXGA, SXGA+
- Narrow bus reduces cable size
- PLL requires no external components
- Power down mode
- Low Profile 64 Lead TQFP Package
- 345mV swing LVDS devices for low EMI
- Supports 200mV Differential Amplitude Outputs
- Pin Compatible with THine THC63LVD103

Block Diagram



Pin Configuration



Pin Description

Pin Name	No of Pin	I/O	Pin Description
TxIN	35	IN	LVC MOS Data Inputs
TxOUT+	5	OUT	Positive LVDS Differential Data Outputs
TxOUT-	5	OUT	Negative LVDS Differential Data Outputs
TxCLKIN	1	IN	LVC MOS Level Clock Input
TxCLKOUT+	1	OUT	Positive LVDS Differential Clock Output
TxCLKOUT-	1	OUT	Negative LVDS Differential Clock Output
Power Down	1	IN	H: Normal Operation L: Power Down (All Outputs are Hi-Z)
R_F	1	IN	Programmable Strobe Select H: Rising Edge, L: Falling Edge
SS	1	IN	Programmable Differential Amplitude Voltage Select H: 345mV, L: 200mV
Vcc / GND	2/5	IN	Power Supply/Ground Pins for LVC MOS Inputs
PLL Vcc / PLL GND	1/1	IN	Power Supply/Ground Pins for PLL
LVDS Vcc / LVDS GND	1/3	IN	Power Supply/Ground Pins for LVDS Outputs

Absolute Maximum Ratings

Supply Voltages	-0.3V to +4V
LVC MOS Input Voltage	-0.3V to (V _{CC} +0.3V)
LVDS Driver Output Voltage	-0.3V to (V _{CC} +0.3V)
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150 °C
Storage Temperature	-65 °C to +150 °C
Lead Temperature (Soldering, 4sec)	+260 °C
Maximum Power Dissipation Capacity (25°C)	1.4 W

Electrical Characteristics
1. LVC MOS DC Specification

 V_{CC}=3.0V to 3.6V Ta=-10°C to 70°C

Symbol	Parameter	Conditions	min	typ	max	unit
V _{IH}	High Level Input Voltage		2.0		V _{CC}	V
V _{IL}	Low Level Input Voltage		GND		0.8	
I _{PD}	Pull Down Current	$\overline{R_F}$ pin, V _{IH} =V _{CC}			100	μA
I _{IN}	Input Current	V _{IN} =V _{CC} , GND, 2.5V or 0.4V			100	

2. LVDS DC Specification

 V_{CC}=3.0V to 3.6V Ta=-10°C to 70°C

Symbol	Parameter	Conditions	min	typ	max	unit	
V _{OD}	Differential Output Voltage	R _L =100 Ohm	SS=V _{CC}	250	345	450	mV
			SS=0V	100	200	300	
ΔV _{OD}	Change in V _{OD} between Complimentary Output states	R _L =100 Ohm			35	mV	
V _{CM}	Common Mode Voltage			1.125	1.25	1.375	V
ΔV _{OS}	Change in V _{OS} between Complimentary Output states					35	mV
I _{OS}	Output Short Circuit Current	V _{OUT} =0V, R _L =100 Ohm			-5	mA	
I _{OZ}	Output Tri-State Current	$\overline{\text{Power Down}}=0V, V_{OUT}=0V \text{ or } V_{CC}$			±10	μA	

3. Transmitter Supply Current

 V_{CC}=3.0V to 3.6V Ta=-10°C to 70°C

Symbol	Parameter	Conditions	min	typ	max	unit	
ICCTW	Transmitter Supply Current	R _L =100Ohm C _L =5pF Worst Case Pattern	f=65MHz		65	77	mA
			f=85MHz		68	80	
ICCTG		R _L =100Ohm C _L =5pF 16Gray Scale Pattern	f=65MHz		50	57	
			f=85MHz		53	60	
ICCTZ		$\overline{\text{Power Down}}=\text{Low}$			10	μA	

4. Switching Characteristics
V_{cc}=3.0V to 3.6V Ta=-10°C to 70°C

Symbol	Parameter	min	typ	max	unit
TCIT	TxCLK IN Transition Time			5	ns
TCIP	TxCLK IN Period	7.41	T	50	
TCIH	TxCLK IN High Time	0.35T	0.5T	0.65T	
TCIL	TxCLK IN Low Time	0.35T	0.5T	0.65T	
LLHT	LVDS Low to High Transition Time		0.6	1.5	
LHLT	LVDS High to Low Transition Time		0.6	1.5	
TCCS	TxOUT Channel to Channel Skew		250		ps
TPP _{os0}	Transmitter Output Pulse Position for Bit 0, f=85MHz	-0.2	0	+0.2	ns
TPP _{os1}	Transmitter Output Pulse Position for Bit 1, f=85MHz	T/7-0.2	T/7	T/7+0.2	
TPP _{os2}	Transmitter Output Pulse Position for Bit 2, f=85MHz	2T/7-0.2	2T/7	2T/7+0.2	
TPP _{os3}	Transmitter Output Pulse Position for Bit 3, f=85MHz	3T/7-0.2	3T/7	3T/7+0.2	
TPP _{os4}	Transmitter Output Pulse Position for Bit 4, f=85MHz	4T/7-0.2	4T/7	4T/7+0.2	
TPP _{os5}	Transmitter Output Pulse Position for Bit 5, f=85MHz	5T/7-0.2	5T/7	5T/7+0.2	
TPP _{os6}	Transmitter Output Pulse Position for Bit 6, f=85MHz	6T/7-0.2	6T/7	6T/7+0.2	
TSTC	TxIN Setup to TxCLK IN	2.5			ns
THTC	TxIN Hold to TxCLK IN	0			
TCCD	TxCLK IN to TxCLK OUT Delay	3.0	3.7	5.5	
TPLLS	Transmitter Phase Lock Loop Set			10	ms
TPDD	Transmitter Power Down Delay			100	ns

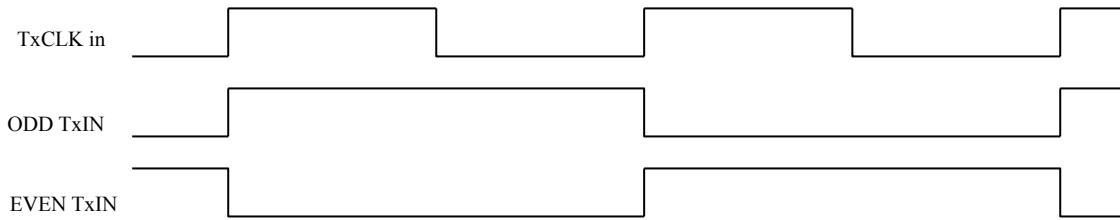


Fig.1 Worst Case Test Pattern

<u>PIN Name</u>	<u>Signal</u>	<u>Signal Pattern</u>	<u>Signal Frequency</u>
TxCLK IN	DOT CLK		f
TxIN28	R0		f/1024
TxIN29	R1		f/512
TxIN21	R2		f/256
TxIN22	R3		f/128
TxIN0	R4		f/64
TxIN1	R5		f/32
TxIN2	R6		f/16
TxIN3	R7		f/8
TxIN4	R8		f/4
TxIN5	R9		f/2
TxIN30	G0		f/1024
TxIN31	G1		f/512
TxIN23	G2		f/256
TxIN24	G3		f/128
TxIN6	G4		f/64
TxIN7	G5		f/32
TxIN8	G6		f/16
TxIN9	G7		f/8
TxIN10	G8		f/4
TxIN11	G9		f/2
TxIN32	B0		f/1024
TxIN33	B1		f/512
TxIN25	B2		f/256
TxIN26	B3		f/128
TxIN12	B4		f/64
TxIN13	B5		f/32
TxIN14	B6		f/16
TxIN15	B7		f/8
TxIN16	B8		f/4
TxIN17	B9		f/2
TxIN27	GND		Steady State, Low
TxIN18	HSYNC		Steady State, High
TxIN19	VSYNC		Steady State, High
TxIN20	DE		Steady State, High
TxIN34	GND		Steady State, Low

Fig.2 “1024-Grayscale” Test Pattern

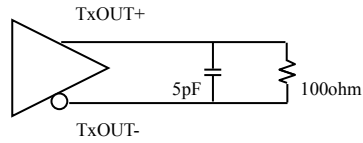


Fig.3: LVDS Output Load

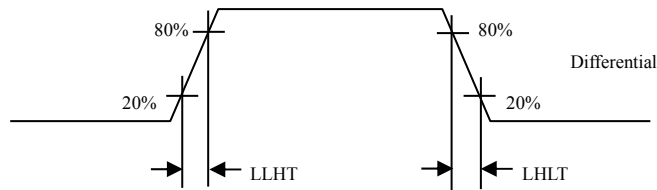


Fig.4: LVDS Transition Times

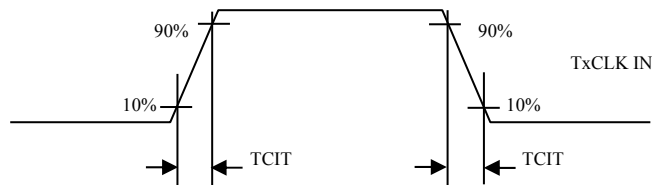


Fig.5: Input Clock Transition Times

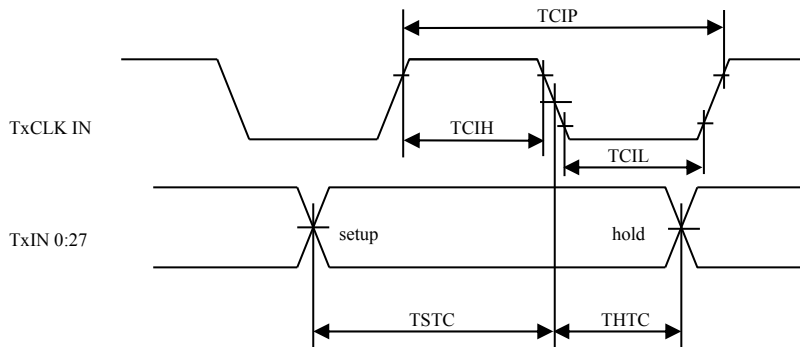


Fig.6: Transmitter Setup/Hold and Low/High Times (Falling Edge Strobe)

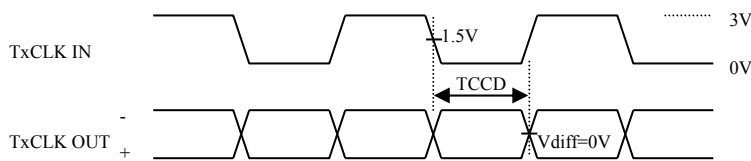


Fig.7: Transmitter Clock in to Clock out Delay (Falling Edge Strobe)

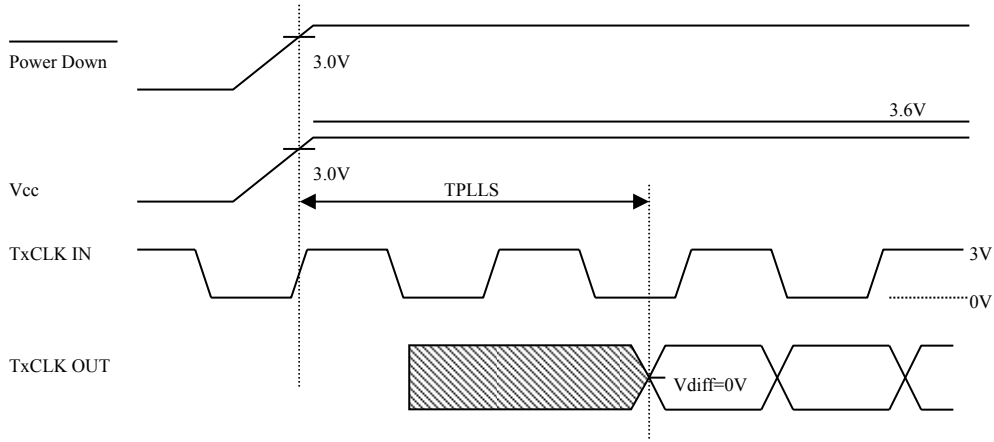


Fig.8: Transmitter Phase Lock Loop Setup Times

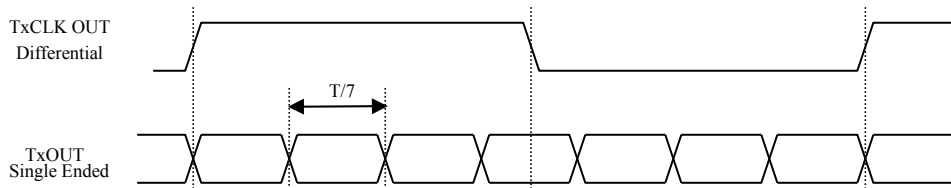


Fig.9: Seven Bits of LVDS in Once Cycle

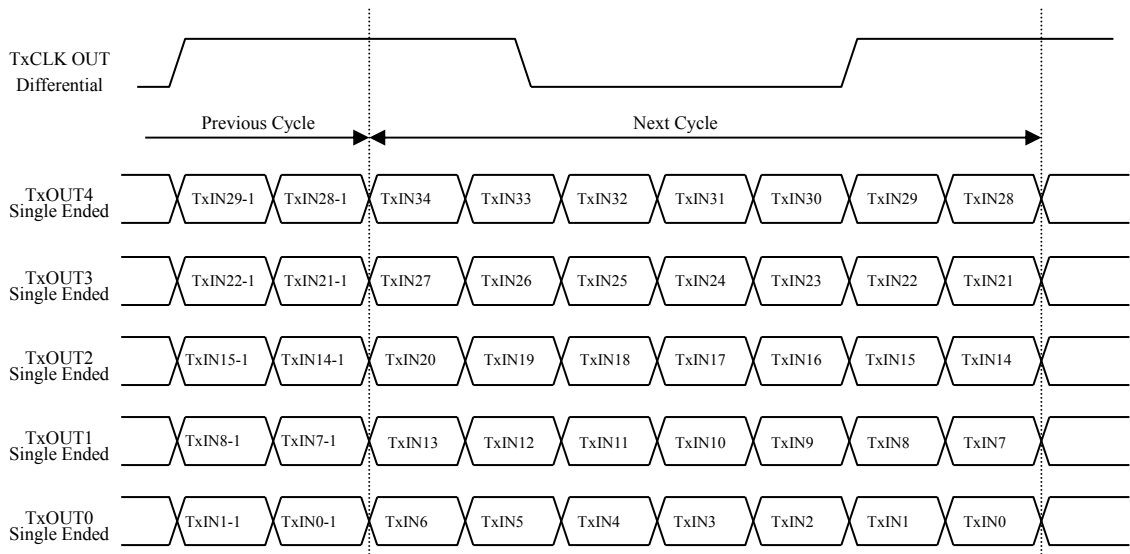


Fig.10: Parallel LVC MOS Data Inputs Mapped to LVDS Outputs

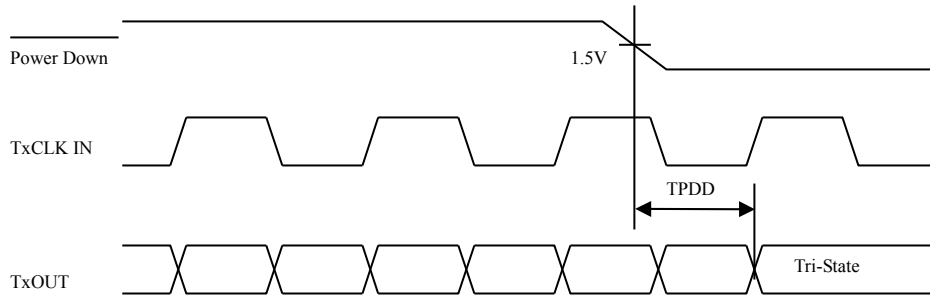


Fig.11: Transmitter Power Down Delay

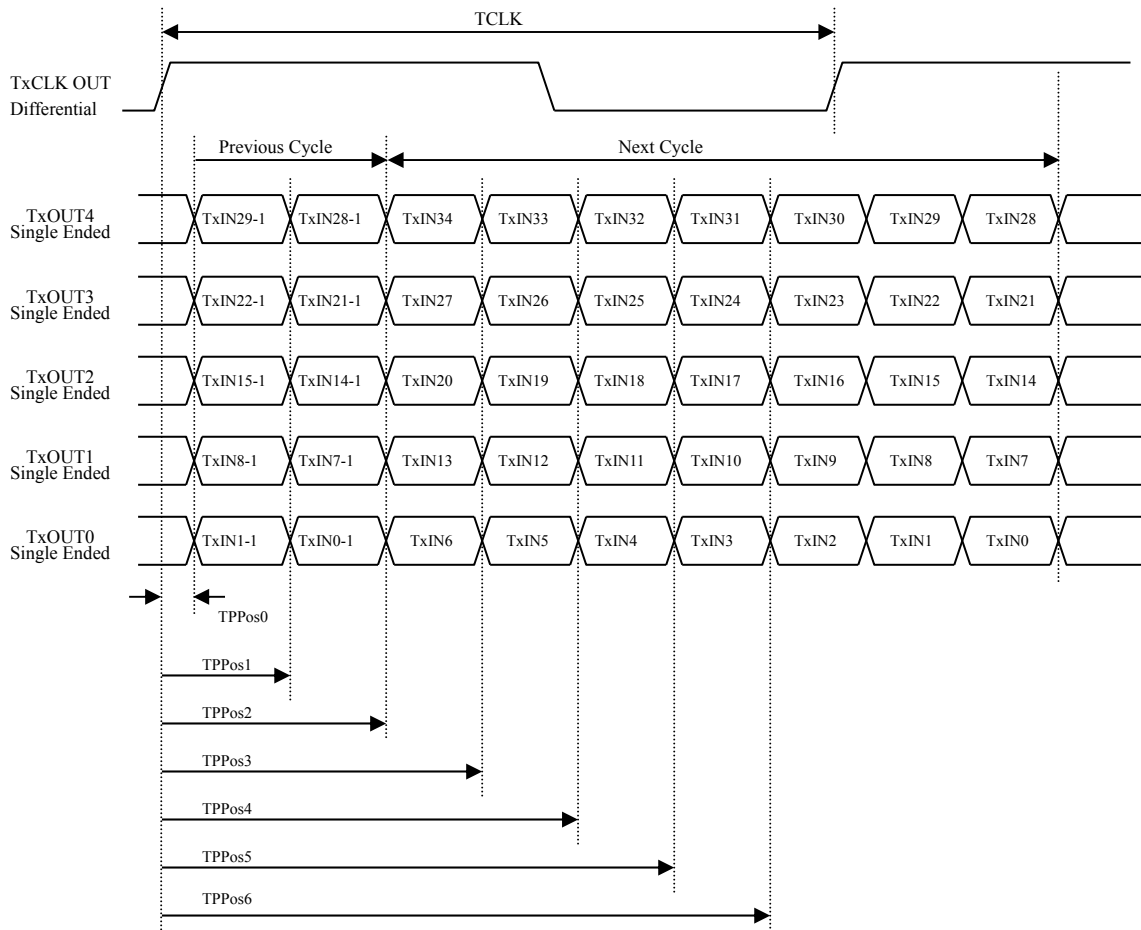
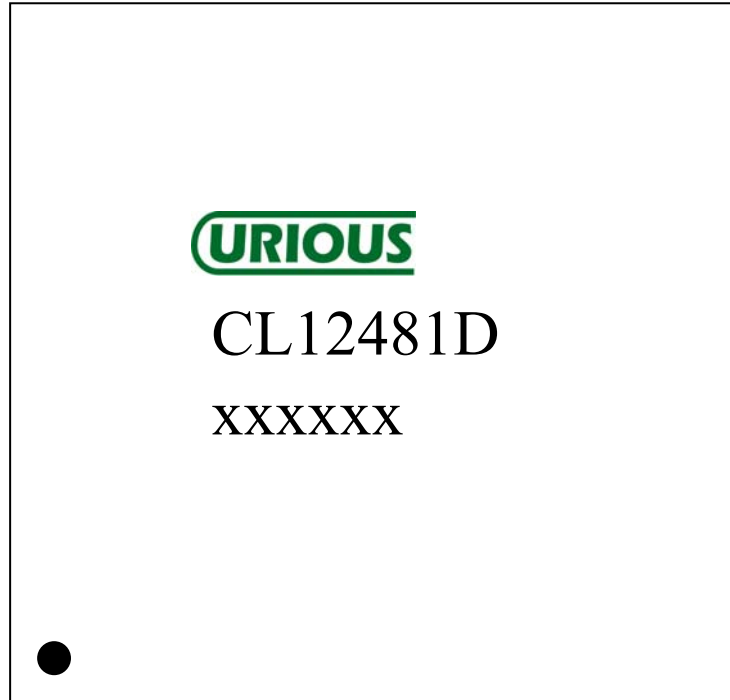


Fig.12: Transmitter LVDS Outputs Pulse Position Measurement



Modification History

Version	Date	Contents
1.00	2010 / 1 / 12	1) Block Diagram changed
0.40	2007 / 7 / 18	1) Output Clock frequency & Data rate added
0.30	2006 / 7 / 25	1) From CL12481C/D to CL12481D changed
0.20	2006 / 5 / 23	1) From CL12481A to CL12481C/D changed 2) SS Mode (200mV Amplitude) added 3) Package LOGO changed 4) Supply Current value changed 5) Maximum Dot Clock Frequency changed 6) Transition Time Changed 7) TxCLKIN Cycle Time Changed
0.10	2005 / 5 / 10	Fig.2 Modified from 16-Gray to 1024-Gray
0.00	2004 / 4 / 27	First Version