Introduction

The CL12491IP270 transmitter is designed to support dual pixel data transmission between Host and Flat Panel Display up to QXGA resolution. The transmitter converts parallel 60bits (Dual Pixel 30-bit color) of LVCMOS data into serial 10-LVDS data streams. Control signals (HSYNC, VSYNC, DE) are sent during blanking intervals. The CL12491IP270 transmitter is an ideal means to solve EMI and cable size problems associated with wide, high-speed CMOS interfaces.

Feature

- 20MHz to 270MHz (max: 340MHz) shift clock support
- Low power single 3.3V (Option: 2.8V) (Option: 1.0 / 1.2 / 1.8V Logic/Level Shifter)
- Clock edge programmable
- Supports VGA, SVGA, XGA, SXGA, UXGA, QXGA
- Supports Dual Link and Single Link
- Supports RGB 18 / 24 / 30
- Narrow bus reduces cable size
- PLL requires no external components
- Power down mode
- 345mV swing LVDS for low EMI
- Supports 200mV Differential Amplitude Outputs

Block Diagram