Introduction

The CL12502IP336 Receiver converts the 3-channnel mini-LVDS serial data streams back to parallel 18bits of LVCMOS (each other 8bit, total 24bits of RGB data). The CL12502IP336 Receiver is an ideal means to solve EMI and cable size problems associated with wide, high speed LVCMOS interface.

Feature

- Input Clock: 60MHz to 336MHz (max: 410MHz)
  Input Data Rate: 120Mbps~672Mbps (max: 810Mbps)
- Output Clock: 20MHz~112MHz (max: 135MHz) shift clock support
- Low power single 3.3V (Option: 2.5 / 2.8V) (Option: 1 / 1.2 / 1.5 / 1.8V Logic/Level Shifter)
- Supports VGA, SVGA, XGA, SXGA , SXGA+
- Narrow bus reduces cable size
- Power down mode
- mini-LVDS format

Block Diagram