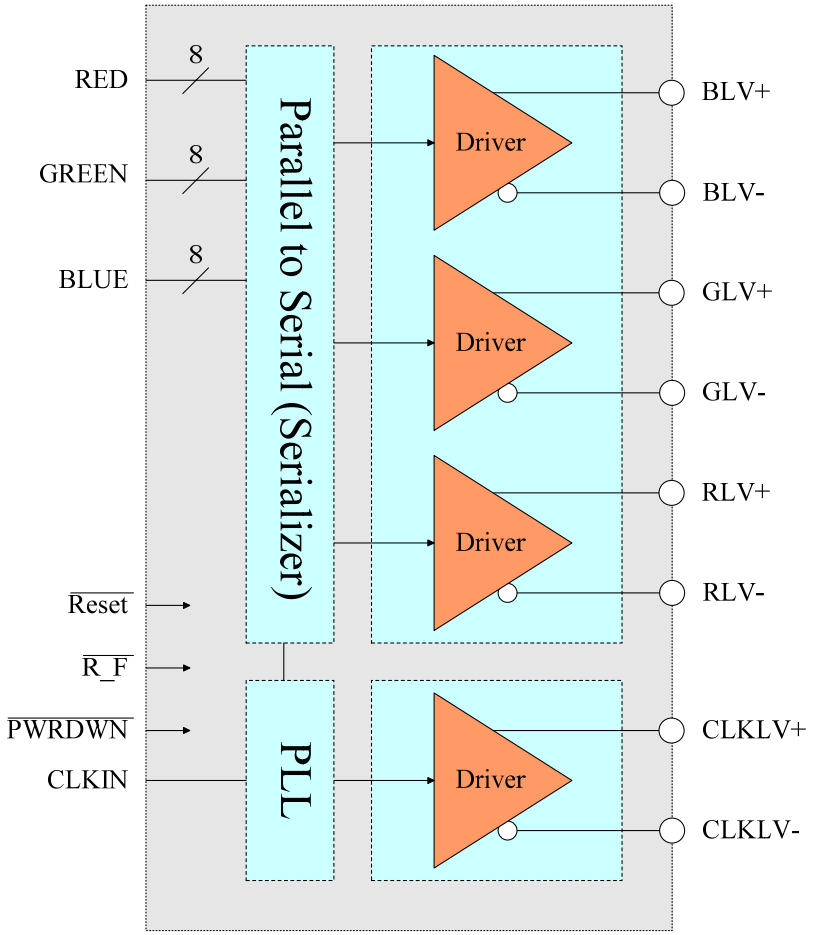
Introduction

The CL12511A340 Transmitter converts 24bits LVCMOS parallel data of RGB into 3-channnel mini-LVDS serial data streams. A Phase-locked transmit clock is transmitter in parallel with the data streams. The CL12511A340 transmitter is programmed for rising edge or falling edge clocks through a dedicated pin. At a transmit clock frequency of 340MHz, 24bits of RGB data are transmitted at a rate of 680Mbps per mini-LVDS data channels. The CL12511A340 Transmitter is an ideal means to solve EMI and cable size problems associated with wide, high speed CMOS interface.

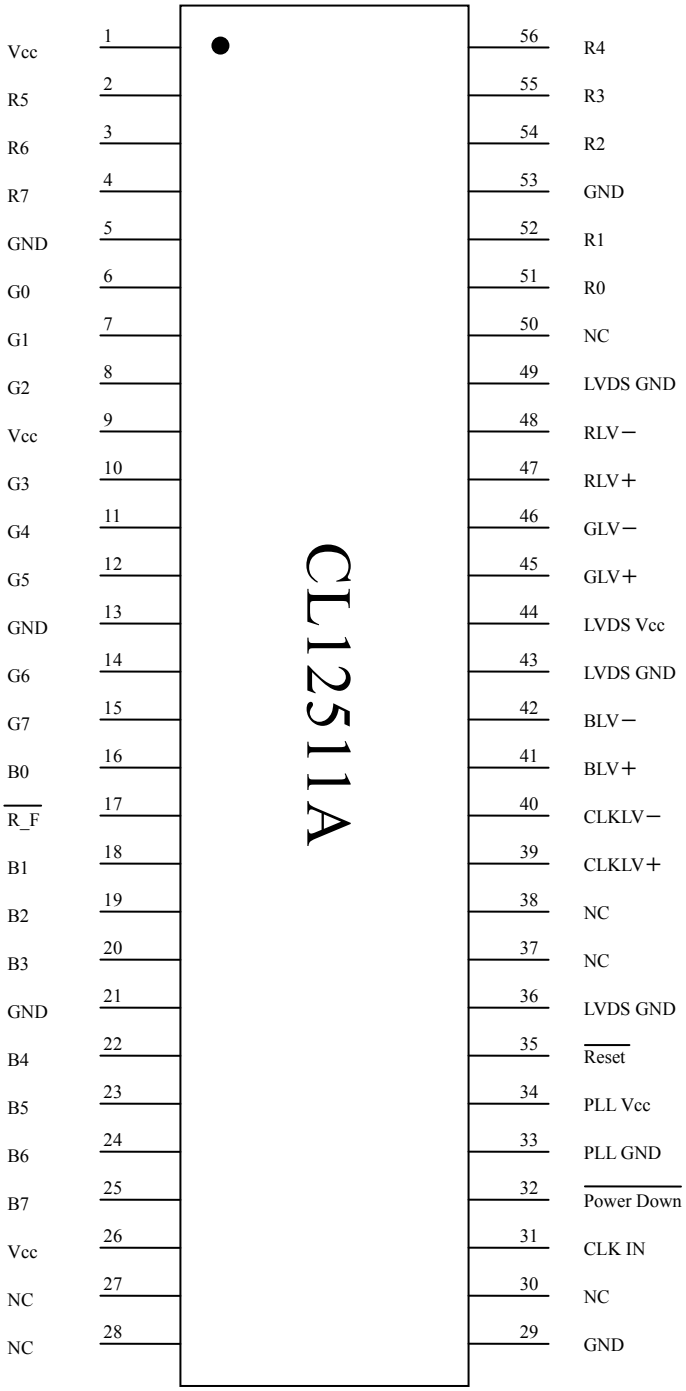
Feature

- Input Clock: 20MHz to 85MHz shift clock support
- Output Clock: 80MHz~340MHz Output Data Rate: 160Mbps~680Mbps
- Low power single 3.3V
- Clock Edge Programmable
- Supports VGA, SVGA, XGA, SXGA, SXGA+
- Narrow bus reduces cable size
- PLL requires no external components
- Power down mode
- Low Profile 56 Lead TSSOP Package
- ±200mV swing mini-LVDS devices for low EMI
- mini-LVDS format

Block Diagram



Pin Configuration



Pin Description

Pin Name	Pin No	I/O	Pin Description
R, G, B<7:0>	24	IN	LVCMOS Data Input
RLV, GLV, BLV+	3	OUT	Positive mini-LVDS Differential Data Out
RLV, GLV, BLV-	3	OUT	Negative mini-LVDS Differential Data Out
CLKIN	1	IN	LVCMOS Level Clock Input
CLKLV+	1	OUT	Positive mini-LVDS Differential Clock Out
CLKLV-	1	OUT	Negative mini-LVDS Differential Clock Out
$\overline{\text{Power Down}}$	1	IN	H: Normal Operation L: Power Down (all Outputs are Hi-Z)
$\overline{\text{R\_F}}$	1	IN	Programmable Strobe Select H: Rising Edge , L: Falling Edge
$\overline{\text{Reset}}$	1	IN	Reset Input H: Normal Operation, L: all “L” Output
Vcc / GND	7/7	IN	Power Supply/Ground Pins for LVCMOS Input
PLL Vcc / GND	1/2	IN	Power Supply/Ground Pins for PLL
mini-LVDS Vcc / GND	1/3	IN	Power Supply/Ground for mini-LVDS Output