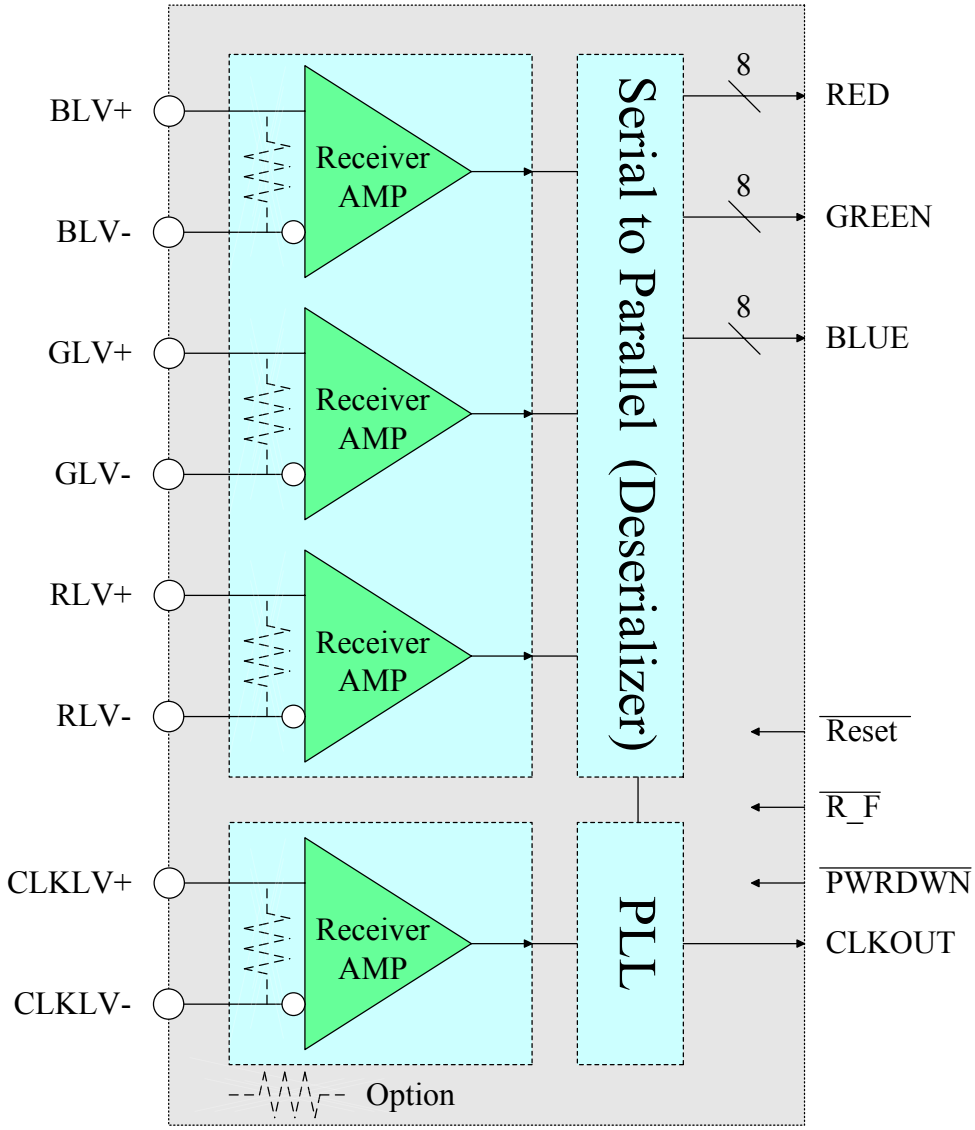
Introduction

The CL12512A340 Receiver converts the 3-channnel mini-LVDS serial data streams back to parallel 24bits of LVCMOS (each other 8bit, total 24bits of RGB data). The CL12512A340 Receiver is an ideal means to solve EMI and cable size problems associated with wide, high speed CMOS interface.

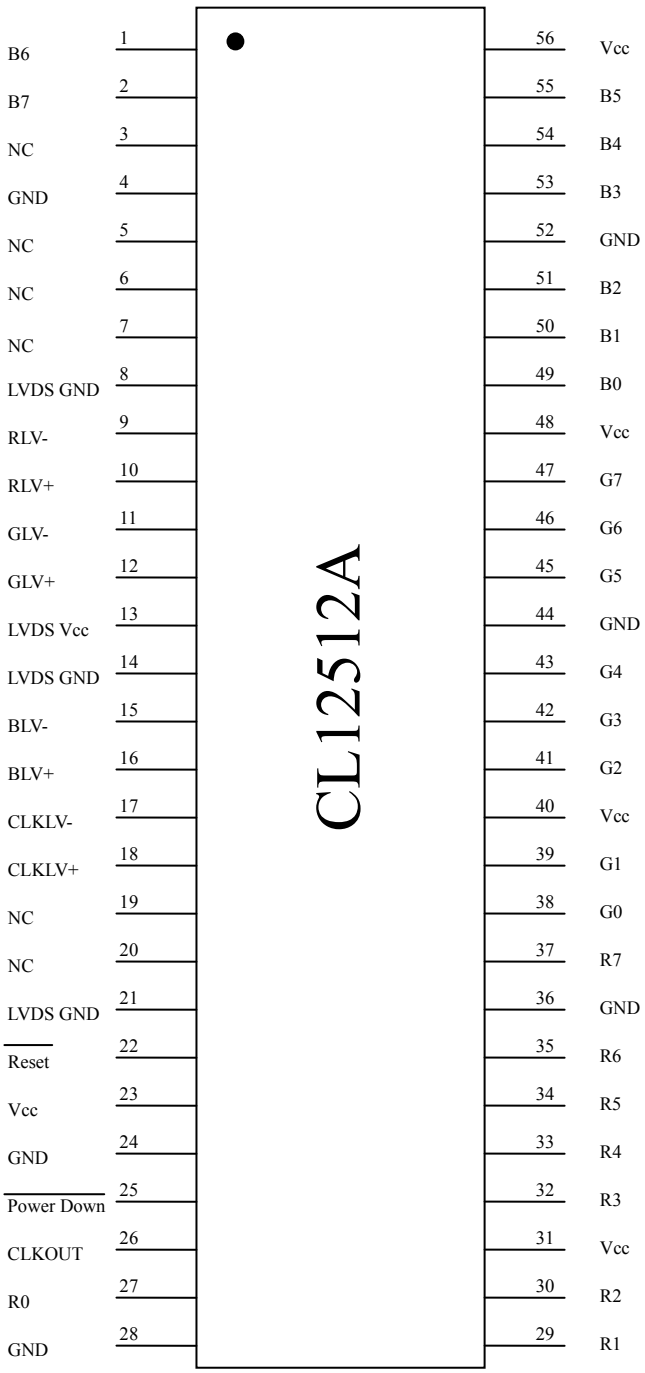
Feature

- Input Clock: 80MHz to 340MHz Input Data Rate: 160Mbps~680Mbps
- Output Clock: 20MHz~85MHz shift clock support
- Low power single 3.3V
- Supports VGA, SVGA, XGA, SXGA , SXGA+
- Narrow bus reduces cable size
- Power down mode
- mini-LVDS format
- Low Profile 56 Lead TSSOP Package

Block Diagram



Pin Configuration



Pin Description

Pin Name	Pin No	I/O	Pin Description
R,G,B<7:0>	24	OUT	LVCMOS Data Output
RLV, GLV, BLV+	3	IN	Positive mini-LVDS Differential Data Input
RLV, GLV, BLV-	3	IN	Negative mini-LVDS Differential Data Input
CLKOUT	1	OUT	LVCMOS Level Clock Output
CLKLV+	1	IN	Positive mini-LVDS Differential Clock Input
CLKLV-	1	IN	Negative mini-LVDS Differential Clock Input
$\overline{\text{Power Down}}$	1	IN	H: Normal Operation L: Power Down (all Output are Pulldown)
$\overline{\text{Reset}}$	1	IN	Reset Input H: Normal Operation, L: all “L” Output
Vcc / GND	3/5	IN	Power Supply/Ground Pins for LVCMOS Outputs
mini-LVDS Vcc / GND	2/4	IN	Power Supply/Ground Pins for mini-LVDS Inputs