Introduction

The CL12611IP340 Transmitter converts 24/32/40/48bits LVCMOS parallel data into 3/4/5/6-channnel sub-LVDS serial data streams. A Phase-locked transmit clock is transmitter in parallel with the data streams. The CL12611IP340 transmitter is programmed for rising edge or falling edge clocks through a dedicated pin. At a transmit clock frequency of 340MHz, 24/32/40/48bits data are transmitted at a rate of 680Mbps per sub-LVDS data channel. The CL12611IP340 Transmitter is an ideal means to solve EMI and cable size problems associated with wide, high speed CMOS interface.

Feature

- Input Clock: 20MHz to 85MHz shift clock support
- Output Clock: 80MHz~340MHz Output Data Rate: 160Mbps~680Mbps
- Low power single 2.8~3.3V (Option: 1.2 / 1.8 / 2.5V) (Option: 1.0 / 1.2 / 1.8V Logic/Level Shifter)
- Clock Edge Programmable
- Narrow bus reduces cable size
- PLL requires no external components
- ±150mV swing sub-LVDS for low EMI
- sub-LVDS DDR format

Block Diagram