Introduction

The CL12612IP340 Receiver converts the 3/4/5/6-channnel sub-LVDS serial data streams back to parallel 24/32/40/48bits of LVCMOS. The CL12612IP340 Receiver is an ideal means to solve EMI and cable size problems associated with wide, high speed CMOS interface.

Feature

- Input Clock: 80MHz to 340MHz Input Data Rate: 160Mbps~680Mbps
- Output Clock: 20MHz~85MHz shift clock support
- Low power single 1.8V (Option: 2.5 / 2.8 / 3.3V) (Option: 1.0 / 1.2 / 1.8V Logic/Level Shifter)
- Narrow bus reduces cable size
- Power down mode
- sub-LVDS DDR format

Block Diagram