Introduction

The CL12616IP325 is sub-LVDS Parallel Receiver optimized for high data rate and low power applications. The CL12616IP325 is designed to support data rates in excess of 650Mbps utilizing sub Low Voltage Differential Signaling (sub-LVDS) technology. The CL12616IP325 accept low voltage (150mV typical) differential input signals and translates them to CMOS output levels.

Feature

- Max 325MHz/650Mbps switching rates
- Low power single 1.8V or 2.8/3.3V (Option: 1.0 / 1.2 V Logic/Level Shifter)
- SMIA CCP Class 0-2 and MIPI CSI compliant
- Power Down Mode ~1uA

Block Diagram