Introduction

The CL12663IP is an ideal means to link mobile camera modules to baseband processers and baseband processers to LCD panels. The CL12663IP is designed to support data rate in excess of 1G/650M/680Mbps utilizing MIPI-DPHY and SMIA, DDR. The differential outputs provide low EMI with its typical low output swing of 150/200mV.

Feature

- ■ Parallel Clock: 20MHz~125MHz shift clock support
- ■ Serial Clock: 80MHz~500MHz, Serial Data rate: 160Mbps~1Gbps
- ■ MIPI-DPHY Ver.1.00.00 / SMIA CCP Class0, 1, 2 compliant
- ■ SMIA CCP Class0, CCP Class1, 2 supports (CLS pin)
- ■ MIPI-DPHY / SMIA / DDR Format support (MDS pin)
- ■ High Speed Rate

Parallel:		~125MHz (CLKI/CLKO0~ n, DI/DO0~n<7:0>)
Serial:	MIPI-DPHY	~1Gbps (Data0~n+/-, Clk+/-)
	SMIA CCP Class0	~208Mbps (Data0~n+/-, Clk+/-)
	SMIACCP Class1, 2	208~650Mbps (Data0~n+/-, Strb+/-)
	DDR Format	~680Mbps (Data0~n+/-, Clk+/-)

- ■ 1.8V (Option: 2.8/3.3v) supply voltage (Option: 1.0 / 1.2 / 1.8v Logic/Level Shifter)
- ■ Clock Edge Programmable (R_F pin)
- ■ MSB/LSB Programmable (SBS pin)
- ■ ±150/200mV swing differential signal for low EMI
- ■ Power Down Mode ~1μA (PD pin)

Block Diagram