Introduction

The CL12683M4T3AM6AIP is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to Host System. The CL12683M4T3AM6AIC is designed to support data rate in excess of maximum 1Gbps utilizing sub-LVDS / mini-LVDS / LVDS / HiSPi(SLVS-400) / MIPI-DPHY / CMOS interface specification. The CL12683M4T3AM6AIP can change Interface type to same PAD for changing mode.

Feature

- MIPI DPHY v1-1 / MIPI CSI / TIA/EIA-644 LVDS / SLVS-400 compliant
- Differential signal of almost CIS serial outputs support
  - 1) sub-LVDS Serial / Parallel
  - 2) mini-LVDS (Reduce Mode LVDS)
  - 3) LVDS
  - 4) HiSPi (SLVS-400)
  - 5) MIPI DPHY (Maximum 4-Lane)
  - 6) CMOS 1.8V (Maximum 10MHz)
- Input Clock Frequency: ~125MHz Input Data Rate: ~250Mbps
- Output Clock Frequency: ~500MHz Output Data Rate: ~1Gbps
- Power Voltage: Single 1.8V
- Maximum Serial Input Ports(Lanes): Clock 1-port / Data 4-ports (lanes)
- Input Serial Clock Edge Programmable for FRPCK pin
- Input Format 2/4/8bit Selectable for BTSEL[1:0]
- MSB/LSB Selectable for SBSEL pin
- Power Consumption: (Process: FF, Temperature: 125, Power Voltage: max) $I_{TOTAL}=V_{CC}+V_{DD}$
  - Active maximum 100mA
  - Sleep maximum 10uA (for PWDN_ALL pin)
- ESD (HBM / MM / CDM / Latch Up): 2kV / 200V / 500V / 100mA