Introduction

The CL12832M12LRM2AM2DIP2500 is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to ISP (Imaging Signal Processer) and DSP. The CL12832M12LRM2AM2DIP2500 is designed to support data rate in excess of maximum 2.5Gbps utilizing SLVS-EC / sub-LVDS interface specification. The CL12832M12LRM2AM2DIP2500 can change Interface type to same PAD for changing mode.

Feature

- SLVS-EC ver.1.2 compliant
- Supporting for two kind Differential Input Signals
  1) SLVS-EC (Maximum 2.5Gbps)
  2) sub-LVDS (Maximum 650Mbps)
- Xtal Input Clock Frequency Selectable 24MHz / 72MHz
- Maximum Input Clock Frequency ~1.25GHz, Maximum Input Data Transfer Rate ~2.5Gbps
- Maximum Output Clock Frequency ~250MHz
- Power Supply : Vcc=1.8V (IO and Analog) Vdd=0.9V (Inside Core)
- Maximum Lane Number : 12-Lane
- 10-bit / Lane Parallel Outputs(SLVS-EC), 2-bit / Lane Parallel Outputs(sub-LVDS)
- Including Power Down Mode
- Including Z-Impedance Detect Circuit
- Consumption Current (Condition Process: FF, Temperature: -40-degree, Supply Voltage: Maximum)
  Maximum Operation Current: Total: 226.8mA
  Maximum Power Down Current: 10uA
- Layout Size:
  （Not Including ESD IO Cell and Including 2nd ESD Cell）
  2518.750 um × 1750.00 um (Before Shrink)
  2266.875 um × 1575.00 um (After Shrink)
- TSMC 28nm HPM/HPC Process (Using of Standard Vth Transistor)
- Supporting Link-layer for CD12822S8LRM2AIP2500 (SLVS-EC link and CSI2/1 Combo) soft macro