Introduction

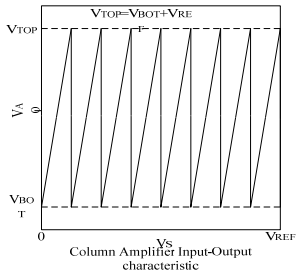
Major of CMOS Image Sensor (CIS) column A/D converter is integrating A/D converter, but it has limited to be high-bits. The CI00101IP can realize 14bits column A/D converter by little increase in a circuit scale for use of "Warp & Walk (Successive Approximation & Single Slope)" algorithm.

Feature

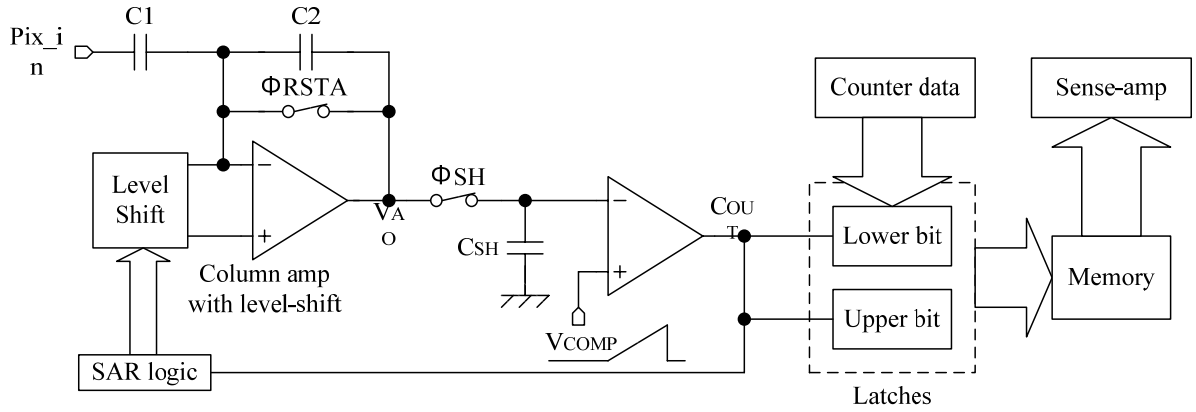
- ■ Power Voltage : 3.3V Analog, 1.8V Analog/Digital Power Supply
- ■ Internal Clock : 108MHz
- ■ A/D Format : CURIOUS Warp & Walk format (Successive Approximation & Single Slope)
- ■ A/D Resolution : 14bit
- ■ A/D Conversion Time : 30usec
- ■ Power Consumption : 20uW
- ■ Column Pitch : About 7um
- ■ V-FPN is nothing and random noise is small, to use High-Gain amplifier for first stage.

Operating Principle and Equivalent Circuit

- ■ High-Gain first amplifier be shift output voltage it did for input signal, and it convert upper level from analog to digital with output saturation prevention.(Right Figure)
- ■ Low level use integrating A/D converter.
- ■ To have redundant in Integrating A/D range can shorten and it can measure High level A/D 1-LSB.
- ■ Offset of column amplifier can be canceled for Digital-CDS or analog-CDS of latter stage.



Column Amplifier Input-Output characteristic



High resolution Column A/D converter Equivalent Circuit

Finished Development Sensor Specification and Realistic Specification

	Finished Development	Realistic	Comments
Power Supply	3.3V/1.8V	2.8V/1.8V	Digital Power is based by devices specification.
Column Pith	7.2um	4.5um	It depends for design-rule of Cap, Wire.
A/D Convert Time	30usec	16usec	High-speed operation is much more possible by increase in current consumption.
Internal Clock Rate	108MHz	250MHz	
Power Consumption	20u	25uW	Include Current Supply of Pixel Readout.