Introduction

The CI00201IP is CMOS Image Sensor A/D Convertor of Column/Parallel readout format. Speeding up and High resolution It can speed up and higher resolution by use of our "W-SA (Double Successive Approximation)"algorithm. It can realize high-quality image for analog amplification by PGA (Programmable Gain Amp) and FPN (Fixing Pattern Noise) decrease by use of Digital CDS (Correlated Double Sampling) between column to column.

Feature

- ■ Process : 0.18um CIS Process (90nm CIS Process)
- ■ Power Voltage : 3V Analog, 1.8V Analog/Digital Power Supply
- ■ A/D Format : CURIOUS W-SA (Double Successive Approximation) format
- ■ A/D Resolution : 12-bit
- ■ A/D Conversion Time : 3.75µsec / Column
- ■ Power Consumption : 40uW / Column Circuit
- ■ Column Pitch : 5.6um
- ■ Noise Reduction : Digital CDS
- ■ PGA Gain : 0, 6, 12, 18dB

Block Diagram