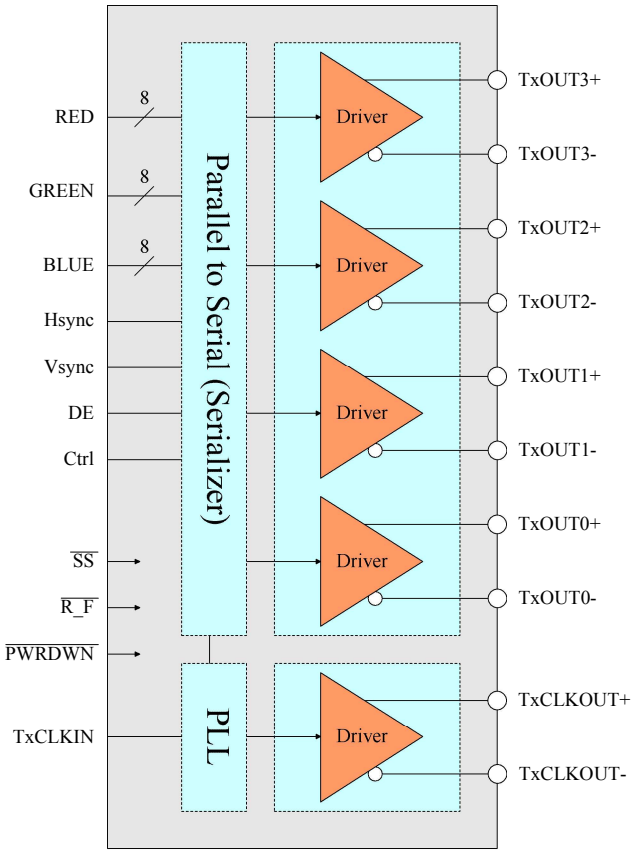
Introduction

The CL12463C transmitter converts parallel 28bits (24bits of RGB data and 4bits of HSYNC, VSYNC, DE and Control) of LVCMOS parallel data into serial four LVDS data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. The CL12463C transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin. At a transmit clock frequency of 85MHz, 24bits of RGB data and 4bits of LCD timing and control data (HSYNC, VSYNC, DE, Control1) are transmitted at a rate of 595Mbps per LVDS data channel. The CL12463C transmitter is an ideal means to solve EMI and cable size problems associated with wide, high-speed CMOS interfaces.

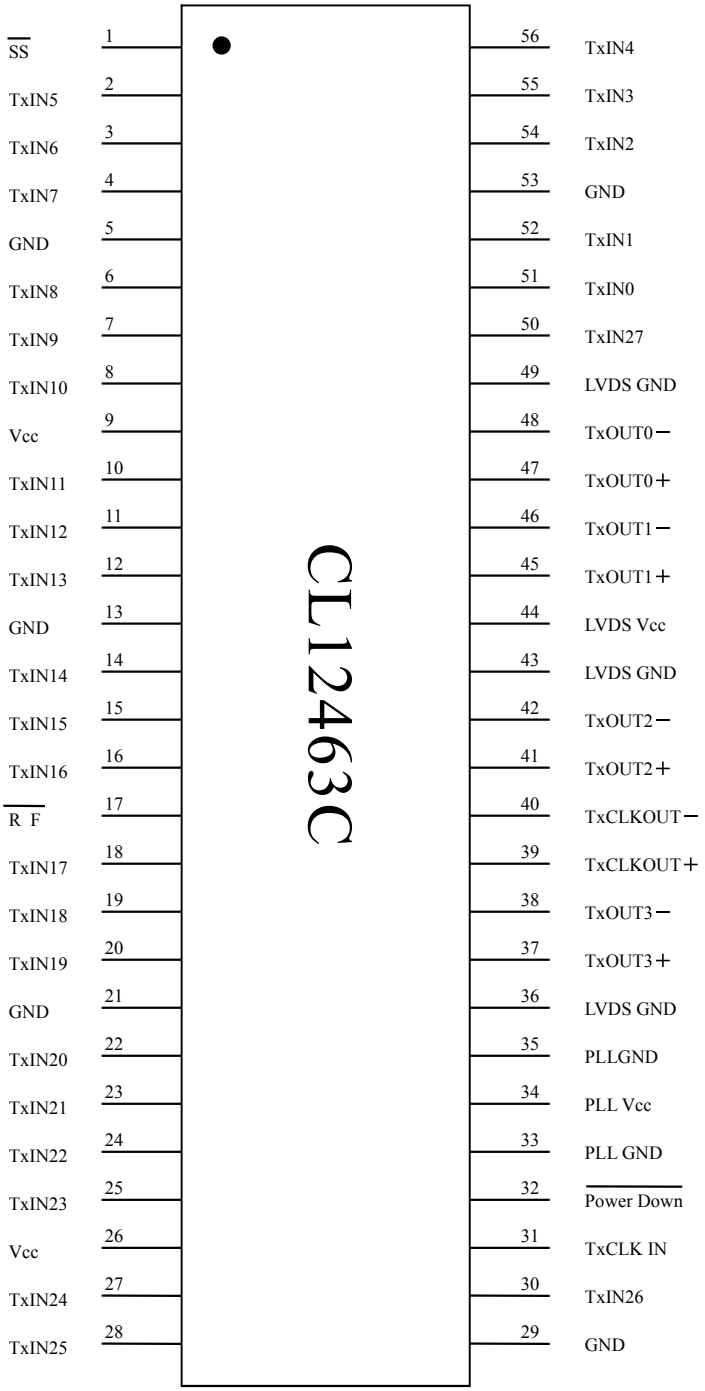
Feature

- Input Clock: 20MHz to 85MHz shift clock support
- Output Clock: 20MHz~85MHz Output Data Rate: 140Mbps~595Mbps
- Low power single 3.3V
- Clock edge programmable
- Supports VGA, SVGA, XGA, SXGA, SXGA+
- Narrow bus reduces cable size
- PLL requires no external components
- Power down mode
- Low Profile 56 Lead TSSOP Package
- 345mV swing LVDS devices for low EMI
- Supports 200mV Differential Amplitude Outputs
- Pin Compatible with DS90C383/385, THC63LVDM83R

Block Diagram



Pin Configuration



Pin Description

Pin Name	No of Pin	I/O	Pin Description
TxIN	28	IN	LVCMOS Data Inputs
TxOUT+	4	OUT	Positive LVDS Differential Data Outputs
TxOUT-	4	OUT	Negative LVDS Differential Data Outputs
TxCLKIN	1	IN	LVCMOS Level Clock Input
TxCLKOUT+	1	OUT	Positive LVDS Differential Clock Output
TxCLKOUT-	1	OUT	Negative LVDS Differential Clock Output
$\overline{\text{Power Down}}$	1	IN	H: Normal Operation L: Power Down (all Outputs are Hi-Z)
$\overline{\text{R\_F}}$	1	IN	Programmable Strobe Select H: Rising Edge, L: Falling Edge
$\overline{\text{SS}}$	1	IN	Programmable Differential Amplitude Voltage Select H: 345mV, L: 200mV
Vcc / GND	3/5	IN	Power Supply/Ground Pins for LVCMOS Inputs
PLL Vcc / PLL GND	1/2	IN	Power Supply/Ground Pins for PLL
LVDS Vcc / LVDS GND	2/4	IN	Power Supply/Ground Pins for LVDS Outputs