Introduction

The CL12463IP135 transmitter converts parallel 28bits (24bits of RGB data and 4bits of HSYNC, VSYNC, DE and Control) of LVCMOS parallel data into serial four LVDS data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. The CL12463IP135 transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin. At a transmit clock frequency of 135MHz, 24bits of RGB data and 4bits of LCD timing and control data (HSYNC, VSYNC, DE, Control1) are transmitted at a rate of 945Mbps per LVDS data channel. The CL12463IP135 transmitter is an ideal means to solve EMI and cable size problems associated with wide, high-speed CMOS interfaces.

Feature

- Input Clock: 20MHz to 135MHz (max: 170MHz) shift clock support
- Output Clock: 20MHz~135MHz (max: 170MHz) Output Data Rate: 140Mbps~945Mbps (1.19Gbps)
- Low power single 3.3V (Option: 2.8V) (Option: 1.0 / 1.2 / 1.8V Logic/Level Shifter)
- Clock edge programmable
- Supports VGA, SVGA, XGA, SXGA, SXGA+
- Narrow bus reduces cable size
- PLL requires no external components
- Power down mode
- 345mV swing LVDS for low EMI
- Supports 200mV Differential Amplitude Outputs

Block Diagram