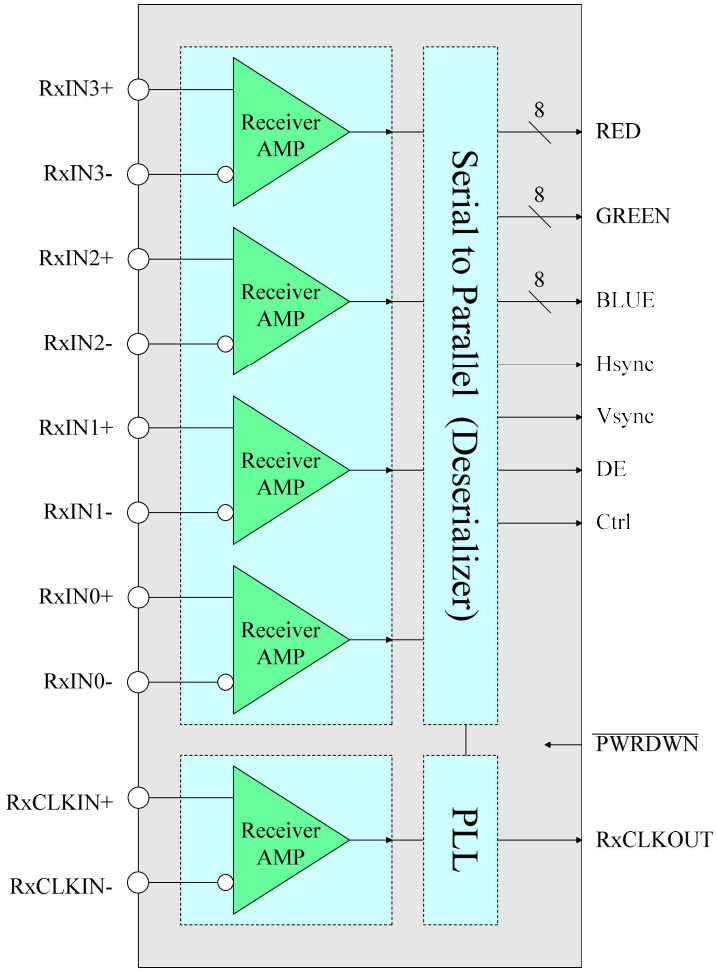
Introduction

The CL12464FF receiver converts serial four LVDS data streams data back into parallel 28bits (24bits of RGB data and 4bits of HSYNC, VSYNC, DE and Control1) of LVCMOS parallel. The CL12464FF receiver' outputs are Falling edge clock. The CL12464FF receiver is an ideal means to solve EMI and cable size problems associated with wide, high-speed LVCMOS interfaces.

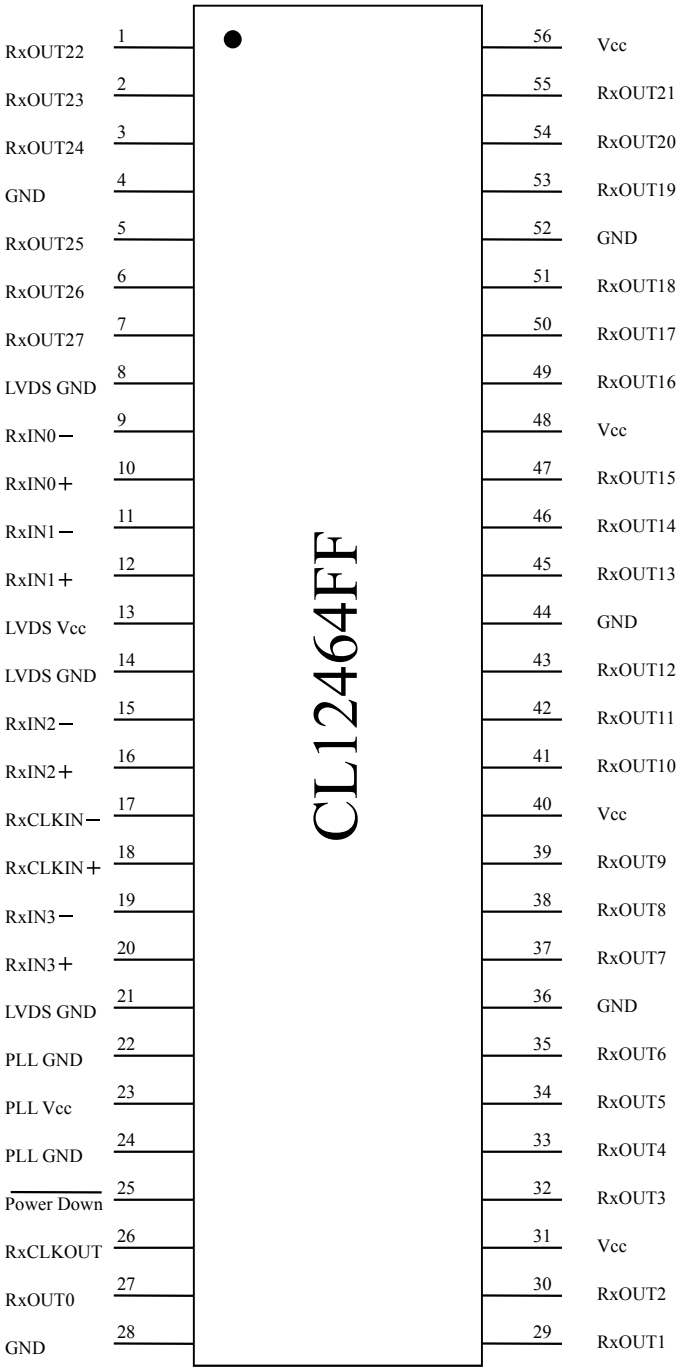
Feature

- Input Clock: 20MHz~85MHz Input Data Rate: 140Mbps~595Mbps
- Output Clock: 20MHz to 85MHz shift clock support
- Low power single 3.3V
- A falling edge strobe
- Supports VGA, SVGA, XGA, SXGA, SXGA+
- Narrow bus reduces cable size
- PLL requires no external components
- Power down mode
- Low Profile 56 Lead TSSOP Package
- 345mV swing LVDS devices for low EMI
- Supports Fail-Safe function to all input channels
- Pin Compatible with DS90C384/386, THC63LVDM84B

Block Diagram



Pin Configuration



Pin Description

Pin Name	No of Pin	I/O	Pin Description
RxOUT	28	OUT	LVCMOS Data Outputs
RxIN+	4	IN	Positive LVDS Differential Data Inputs
RxIN-	4	IN	Negative LVDS Differential Data Inputs
RxCLKOUT	1	OUT	LVCMOS Level Clock Output
RxCLKIN+	1	IN	Positive LVDS Differential Clock Input
RxCLKIN-	1	IN	Negative LVDS Differential Clock Input
$\overline{\text{Power Down}}$	1	IN	H:Normal Operation L:Power Down (all Outputs are Hi-Z)
Vcc / GND	3/5	IN	Power Supply/Ground Pins for LVCMOS Outputs
PLL Vcc / PLL GND	1/2	IN	Power Supply/Ground Pins for PLL
LVDS Vcc / LVDS GND	2/4	IN	Power Supply/Ground Pins for LVDS Inputs

Control Signal Truth Table

$\overline{\text{Power Down}}$	$\overline{\text{R\_F}}$	OE	RxOUT	RxCLKOUT
0	0	0	All Outputs Hi-Z	Output Hi-Z
0	0	1	All ”0” Outputs	”0” Output
0	1	0	All Outputs Hi-Z	Output Hi-Z
0	1	1	All ”0” Outputs	”0” Output
1	0	0	All Outputs Hi-Z	Output Hi-Z
1	0	1	All Data Outputs	Falling Edge
1	1	0	All Outputs Hi-Z	Output Hi-Z
1	1	1	All Data Outputs	Rising Edge