Introduction

The CL12464IP135 receiver converts serial four LVDS data streams data back into parallel 28bits (24bits of RGB data and 4bits of HSYNC, VSYNC, DE and Control1) of LVCMOS parallel. The CL12464IP135 receiver can be programmed for rising edge or falling edge clocks through a dedicated pin. The CL12464IP135 receiver' outputs are Falling edge clock. The CL12464IP135 receiver is an ideal means to solve EMI and cable size problems associated with wide, high-speed CMOS interfaces.

Feature

- Input Clock: 20MHz~135MHz Input Data Rate: 140Mbps~945Mbps
- Output Clock: 20MHz to 135MHz shift clock support
- Low power single 3.3V (Option: 2.8V) (Option: 1.0 / 1.2 / 1.8V Logic/Level Shifter)
- Clock edge programmable
- Supports VGA, SVGA, XGA, SXGA, SXGA+
- Narrow bus reduces cable size
- PLL requires no external components
- Power down mode
- 345mV swing LVDS for low EMI
- Supports Fail-Safe function to all input channels

Block Diagram