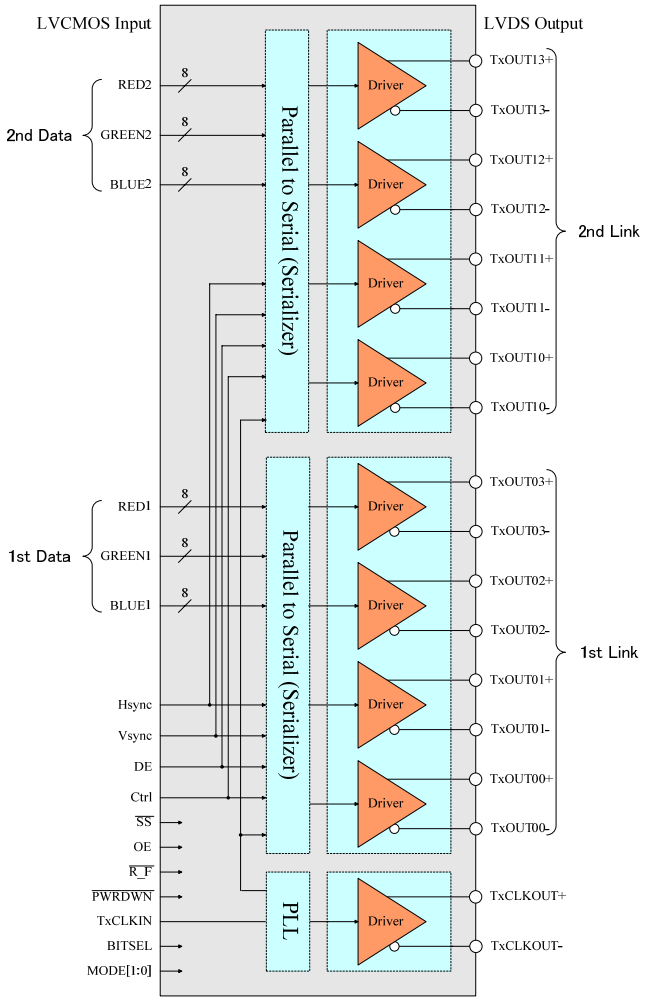
Introduction

The CL12471B transmitter is designed to support dual pixel data transmission between Host and Flat Panel Display up to UXGA resolution. The transmitter converts parallel 48bits (Dual Pixel 24-bit color) of LVCMOS data into serial 8-LVDS data streams. Control signals (HSYNC, VSYNC, DE) are sent during blanking intervals. The CL12471B transmitter is an ideal means to solve EMI and cable size problems associated with wide, high-speed LVCMOS interfaces.

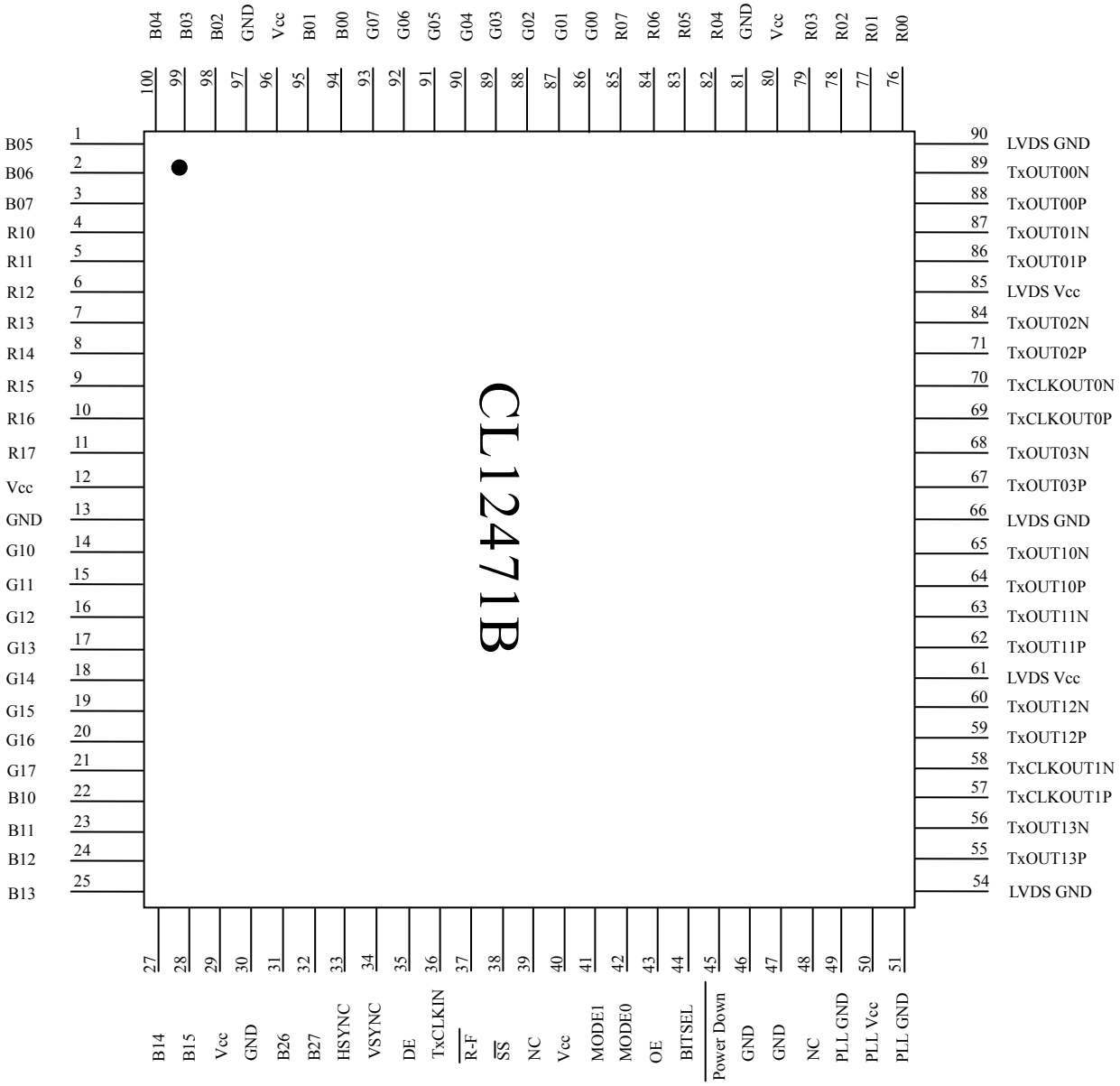
Feature

- 20MHz to 270MHz shift clock support
- Low power single 3.3V
- Clock edge programmable
- Supports VGA, SVGA, XGA, SXGA, UXGA
- Supports Dual Link and Single Link
- Supports RGB 18 / 24
- Narrow bus reduces cable size
- PLL requires no external components
- Power down mode
- Low Profile 100 Lead TQFP Package
- 345mV swing LVDS devices for low EMI
- Supports 200mV Differential Amplitude Outputs
- Pin Compatible with THine THC63LVD823

Block Diagram



Pin Configuration



Pin Description

<table>
<tr><th>Pin Name</th><th>No of Pin</th><th>I/O</th><th>Pin Description</th></tr>
<tr><td>TxOUT00N~03N
TxOUT00P~03P</td><td>8</td><td>OUT</td><td>1st Link LVDS Differential Data Outputs
The 1st pixel output data when Dual Link</td></tr>
<tr><td>TxCLKOUT0N/0P</td><td>2</td><td>OUT</td><td>1st Link LVDS Differential Clock Outputs</td></tr>
<tr><td>TxOUT10N~13N
TxOUT10P~13P</td><td>8</td><td>OUT</td><td>2nd Link LVDS Differential Data Outputs
These pins are disabled when Single Link</td></tr>
<tr><td>TxCLKOUT1N/1P</td><td>2</td><td>OUT</td><td>2nd Link LVDS Differential Clock Outputs</td></tr>
<tr><td>R00~R07
G00~G07
B00~B07</td><td>24</td><td>IN</td><td>1st Pixel LVCMOS Data Inputs</td></tr>
<tr><td>R10~R17
G10~G17
B10~B17</td><td>24</td><td>IN</td><td>2nd Pixel LVCMOS Data Inputs</td></tr>
<tr><td>TxCLKIN</td><td>1</td><td>IN</td><td>LVCMOS Level Clock Input</td></tr>
<tr><td>DE</td><td>1</td><td>IN</td><td>Data Enable Input</td></tr>
<tr><td>VSYNC</td><td>1</td><td>IN</td><td>Vsync Input</td></tr>
<tr><td>HSYNC</td><td>1</td><td>IN</td><td>Hsync Input</td></tr>
<tr><td>OE</td><td>1</td><td>IN</td><td>H: Output Enable
L: Output Disable (All Outputs are Hi-Z)</td></tr>
<tr><td>$\overline{\text{Power Down}}$</td><td>1</td><td>IN</td><td>H: Normal Operation
L: Power Down (All Outputs are Hi-Z)</td></tr>
<tr><td>$\overline{\text{R\_F}}$</td><td>1</td><td>IN</td><td>Programmable Strobe Select
H: Rising Edge, L: Falling Edge</td></tr>
<tr><td>SS</td><td>1</td><td>IN</td><td>Programmable Differential Amplitude Voltage Select
H: 345mV, L: 200mV</td></tr>
<tr><td>MODE0/MODE1</td><td>2</td><td>IN</td><td>Data Mode
<table>
<tr><th>MODE 1</th><th>MODE 0</th><th>Mode</th></tr>
<tr><td>L</td><td>L</td><td>Dual Link (Dual-in/Dual-out)</td></tr>
<tr><td>L</td><td>H</td><td>Not use</td></tr>
<tr><td>H</td><td>L</td><td>Not use</td></tr>
<tr><td>H</td><td>H</td><td>Single Link (single-in/single-out)</td></tr>
</table></td></tr>
<tr><td>BITSEL</td><td>1</td><td>IN</td><td>6bit/8bit Color Select
H: 6bit (TxOUTx3N/x3P…GND) L: 8bit</td></tr>
<tr><td>Vcc / GND</td><td>3/4</td><td>IN</td><td>Power Supply/Ground Pins for LVCMOS Inputs</td></tr>
<tr><td>PLL Vcc / PLL GND</td><td>1/2</td><td>IN</td><td>Power Supply/Ground Pins for PLL</td></tr>
<tr><td>LVDS Vcc / LVDS GND</td><td>2/3</td><td>IN</td><td>Power Supply/Ground Pin for LVDS Outputs</td></tr>
</table>