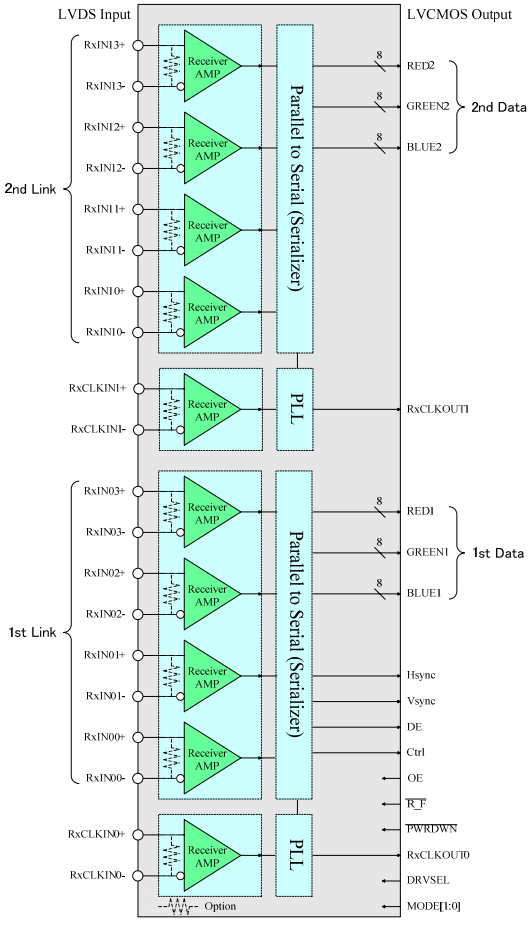
## Introduction

The CL12472B receiver is designed to support dual pixel data transmission between Host and Flat Panel Display up to UXGA resolution. The receiver converts serial 8-LVDS data streams back into parallel 48bits (Dual Pixel 24-bit color) of LVCMOS data. Control signals (HSYNC, VSYNC, DE) are sent during blanking intervals. The CL12472B receiver is an ideal means to solve EMI and cable size problems associated with wide, high-speed LVCMOS interfaces.

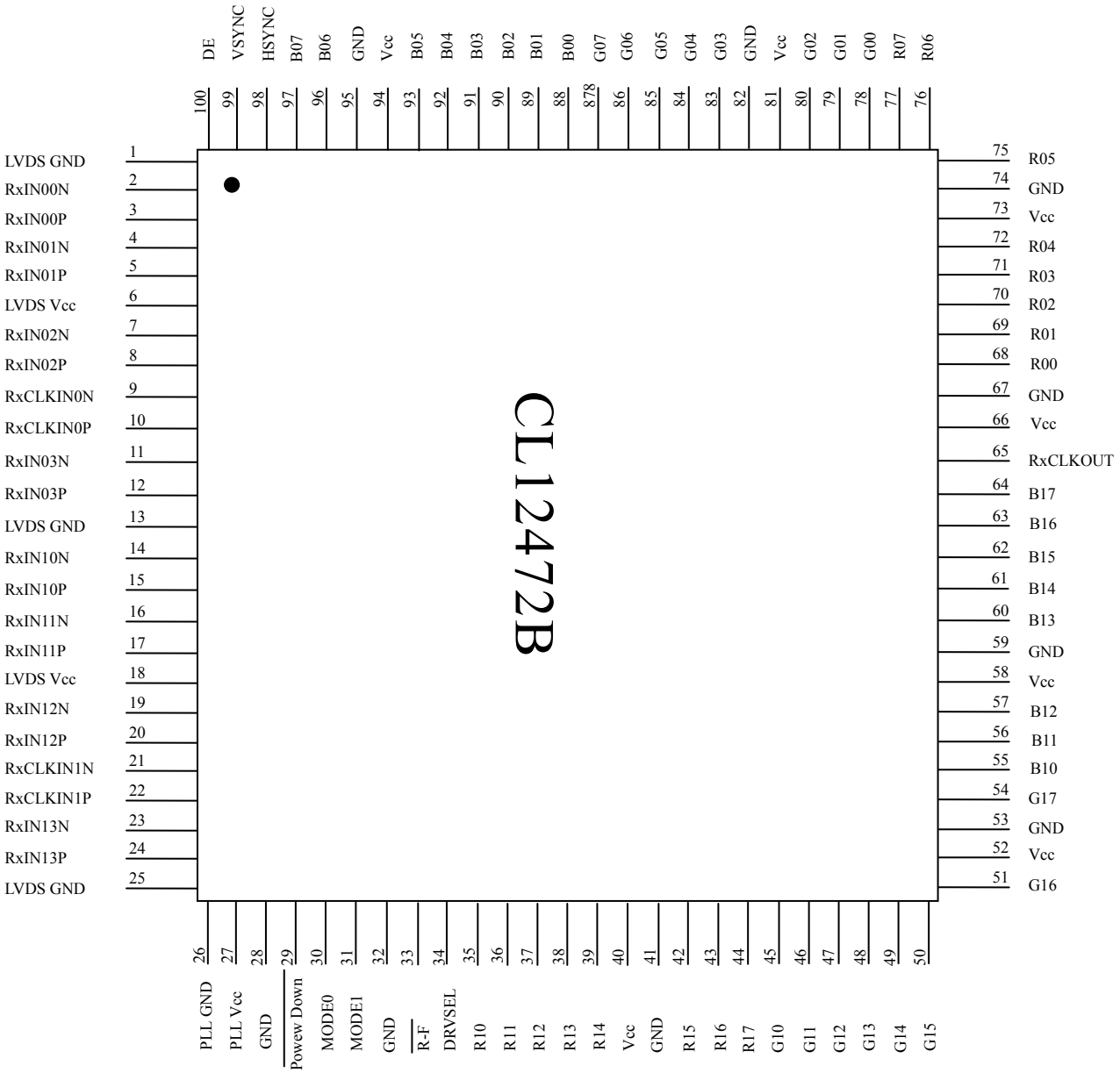
## Feature

- 20MHz to 270MHz shift clock support
- Low power single 3.3V
- Clock edge programmable
- Supports VGA, SVGA, XGA, SXGA, UXGA
- Supports Dual Link and Single Link
- Supports RGB 18 / 24
- Narrow bus reduces cable size
- PLL requires no external components
- Power down mode
- Supports Fail-Safe function to all input channels
- Low Profile 100 Lead TQFP Package
- Pin Compatible with THine THC63LVD824

## Block Diagram



## Pin Configuration



## Pin Description

<table>
<tr><th>Pin Name</th><th>No of Pin</th><th>I/O</th><th>Pin Description</th></tr>
<tr><td>RxIN00N~03N<br>RxIN00P~03P</td><td>8</td><td>IN</td><td>1st Link LVDS Differential Data Inputs<br>The 1st pixel input data when Dual Link</td></tr>
<tr><td>RxCLKIN0N/0P</td><td>2</td><td>IN</td><td>1st Link LVDS Differential Clock Inputs</td></tr>
<tr><td>RxIN10N~13N<br>RxIN10P~13P</td><td>8</td><td>IN</td><td>2nd Link LVDS Differential Data Inputs<br>These pins are disabled when Single Link</td></tr>
<tr><td>RxCLKIN1N/1P</td><td>2</td><td>IN</td><td>2nd Link LVDS Differential Clock Input</td></tr>
<tr><td>R00~R07<br>G00~G07<br>B00~B07</td><td>24</td><td>OUT</td><td>1st Pixel LVCMOS Data Outputs</td></tr>
<tr><td>R10~R17<br>G10~G17<br>B10~B17</td><td>24</td><td>OUT</td><td>2nd Pixel LVCMOS Data Outputs</td></tr>
<tr><td>RxCLKOUT</td><td>1</td><td>OUT</td><td>LVCMOS Level Clock Output</td></tr>
<tr><td>DE</td><td>1</td><td>OUT</td><td>Data Enable Output</td></tr>
<tr><td>VSYNC</td><td>1</td><td>OUT</td><td>Vsync Output</td></tr>
<tr><td>HSYNC</td><td>1</td><td>OUT</td><td>Hsync Output</td></tr>
<tr><td>$\overline{\text{Power Down}}$</td><td>1</td><td>IN</td><td>H: Normal Operation<br>L: Power Down (All Outputs are Hi-Z)</td></tr>
<tr><td>$\overline{\text{R\_F}}$</td><td>1</td><td>IN</td><td>Programmable Strobe Select<br>H: Rising Edge, L: Falling Edge</td></tr>
<tr><td>MODE0/MODE1</td><td>2</td><td>IN</td><td>Data Mode
<table>
<tr><th>MODE 1</th><th>MODE 0</th><th>Mode</th></tr>
<tr><td>L</td><td>L</td><td>Dual Link (Dual-in/Dual-out)</td></tr>
<tr><td>L</td><td>H</td><td>Not use</td></tr>
<tr><td>H</td><td>L</td><td>Not use</td></tr>
<tr><td>H</td><td>H</td><td>Single Link (single-in/single-out)</td></tr>
</table></td></tr>
<tr><td>DRVSEL</td><td>1</td><td>IN</td><td>Output Drivability Select<br>H: High Power, L: Low Power</td></tr>
<tr><td>Vcc / GND</td><td>7/9</td><td>IN</td><td>Power Supply/Ground Pins for LVCMOS Inputs</td></tr>
<tr><td>PLL Vcc / PLL GND</td><td>1/1</td><td>IN</td><td>Power Supply/Ground Pins for PLL</td></tr>
<tr><td>LVDS Vcc / LVDS GND</td><td>2/3</td><td>IN</td><td>Power Supply/Ground Pin for LVDS Outputs</td></tr>
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