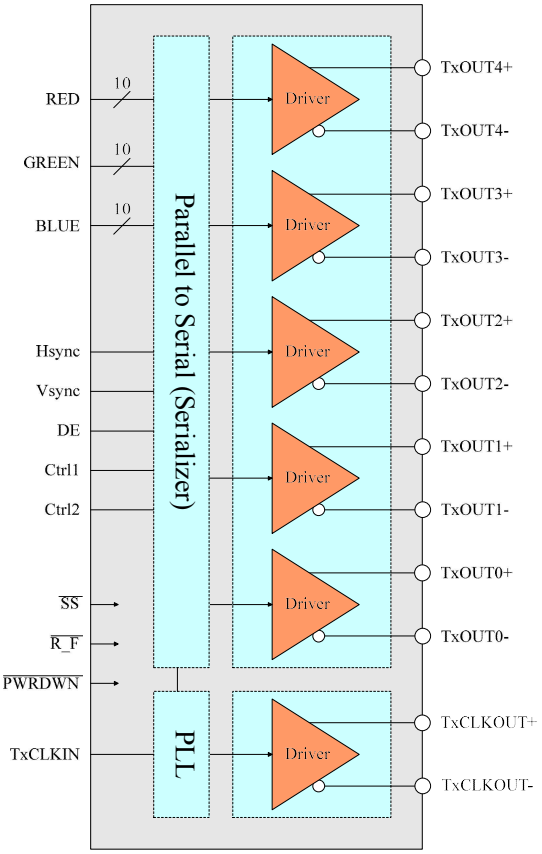
Introduction

The CL12481D transmitter converts parallel 35bits (30bits of RGB data and 5bits of HSYNC, VSYNC, DE and Control1, Control2) of LVCMOS data into serial 5-LVDS data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a sixth LVDS link. The CL12481D transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin. At a transmit clock frequency of 85MHz, 30bits of RGB data and 5bits of LCD timing and control data (HSYNC, VSYNC, DE, Control1, Control2) are transmitted at a rate of 595Mbps per LVDS data channel. The CL12481D transmitter is an ideal means to solve EMI and cable size problems associated with wide, high-speed LVCMOS interfaces.

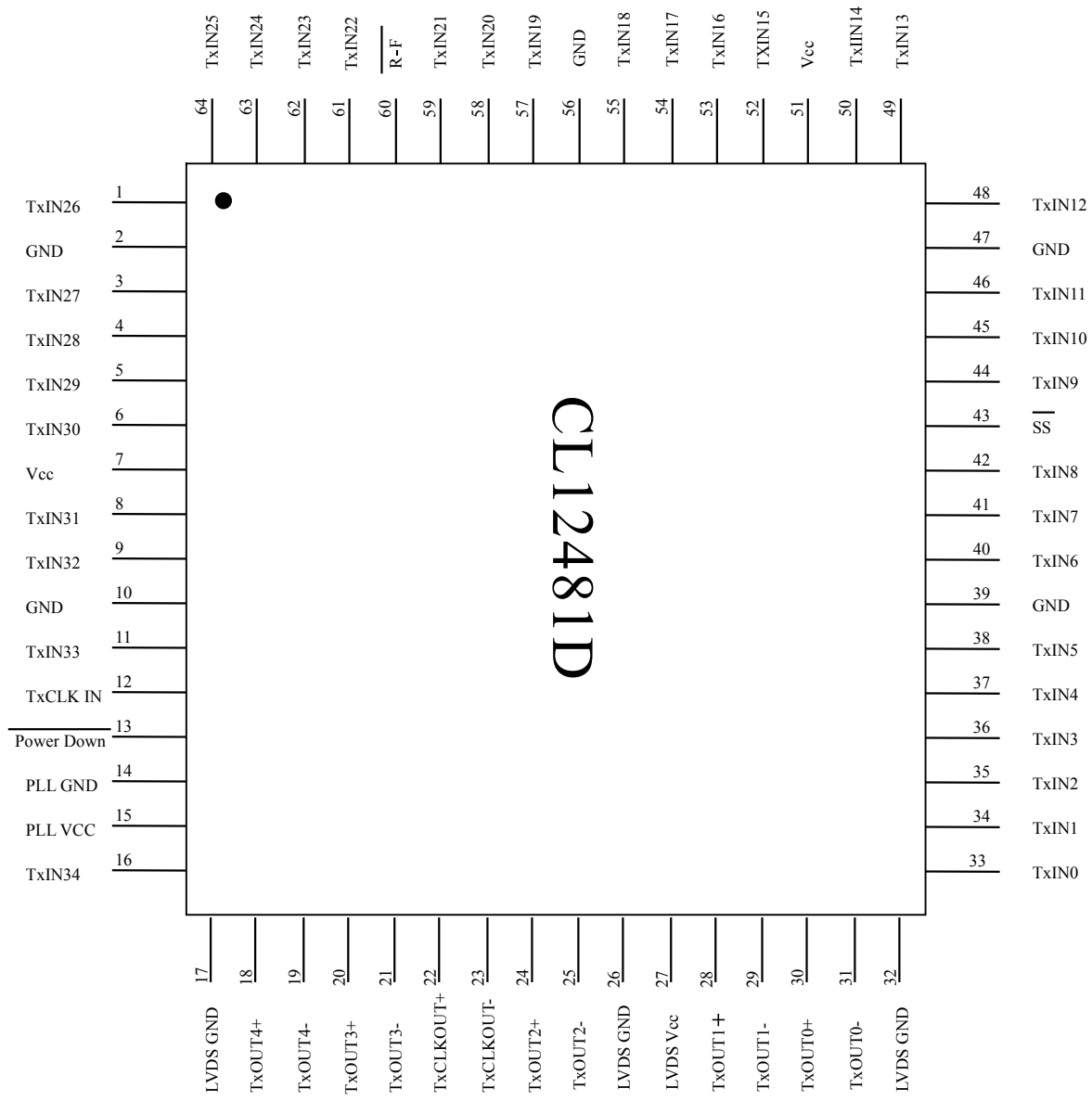
Feature

- Input Clock: 20MHz to 85MHz shift clock support
- Output Clock: 20MHz~85MHz Output Data Rate: 140Mbps~595Mbps
- Low power single 3.3V
- Clock edge programmable
- Supports VGA, SVGA, XGA, SXGA, SXGA+
- Narrow bus reduces cable size
- PLL requires no external components
- Power down mode
- Low Profile 64 Lead TQFP Package
- 345mV swing LVDS devices for low EMI
- Supports 200mV Differential Amplitude Outputs
- Pin Compatible with THine THC63LVD103

Block Diagram



Pin Configuration



Pin Description

Pin Name	No of Pin	I/O	Pin Description
TxIN	35	IN	LVCMOS Data Inputs
TxOUT+	5	OUT	Positive LVDS Differential Data Outputs
TxOUT-	5	OUT	Negative LVDS Differential Data Outputs
TxCLKIN	1	IN	LVCMOS Level Clock Input
TxCLKOUT+	1	OUT	Positive LVDS Differential Clock Output
~~TxCLKOUT-~~	1	OUT	Negative LVDS Differential Clock Output
Power Down	1	IN	H: Normal Operation L: Power Down (All Outputs are Hi-Z)
R_F	1	IN	Programmable Strobe Select H: Rising Edge, L: Falling Edge
SS	1	IN	Programmable Differential Amplitude Voltage Select H: 345mV, L: 200mV
Vcc / GND	2/5	IN	Power Supply/Ground Pins for LVCMOS Inputs
PLL Vcc / PLL GND	1/1	IN	Power Supply/Ground Pins for PLL
LVDS Vcc / LVDS GND	1/3	IN	Power Supply/Ground Pins for LVDS Outputs