

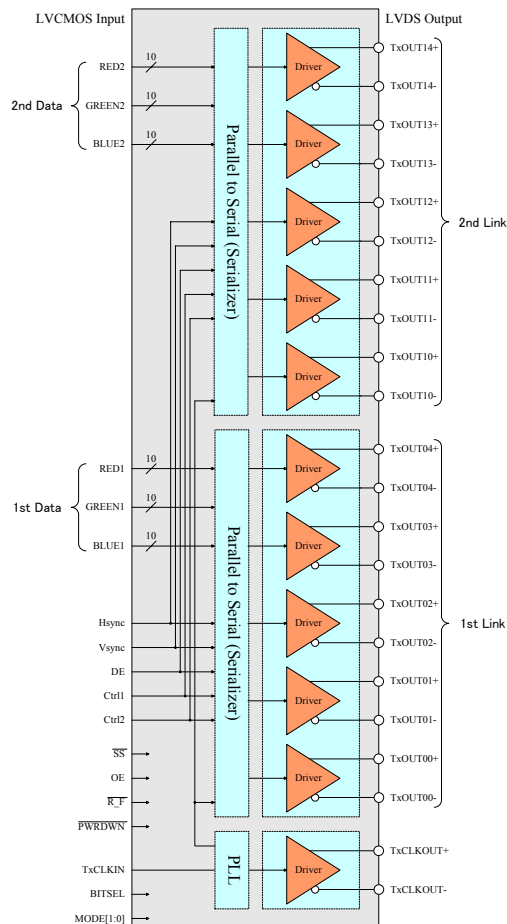
Introduction

The CL12491B transmitter is designed to support dual pixel data transmission between Host and Flat Panel Display up to QXGA resolution. The transmitter converts parallel 60bits (Dual Pixel 30-bit color) of LVCMOS data into serial 10-LVDS data streams. Control signals (HSYNC, VSYNC, DE) are sent during blanking intervals. The CL12491B transmitter is an ideal means to solve EMI and cable size problems associated with wide, high-speed LVCMOS interfaces.

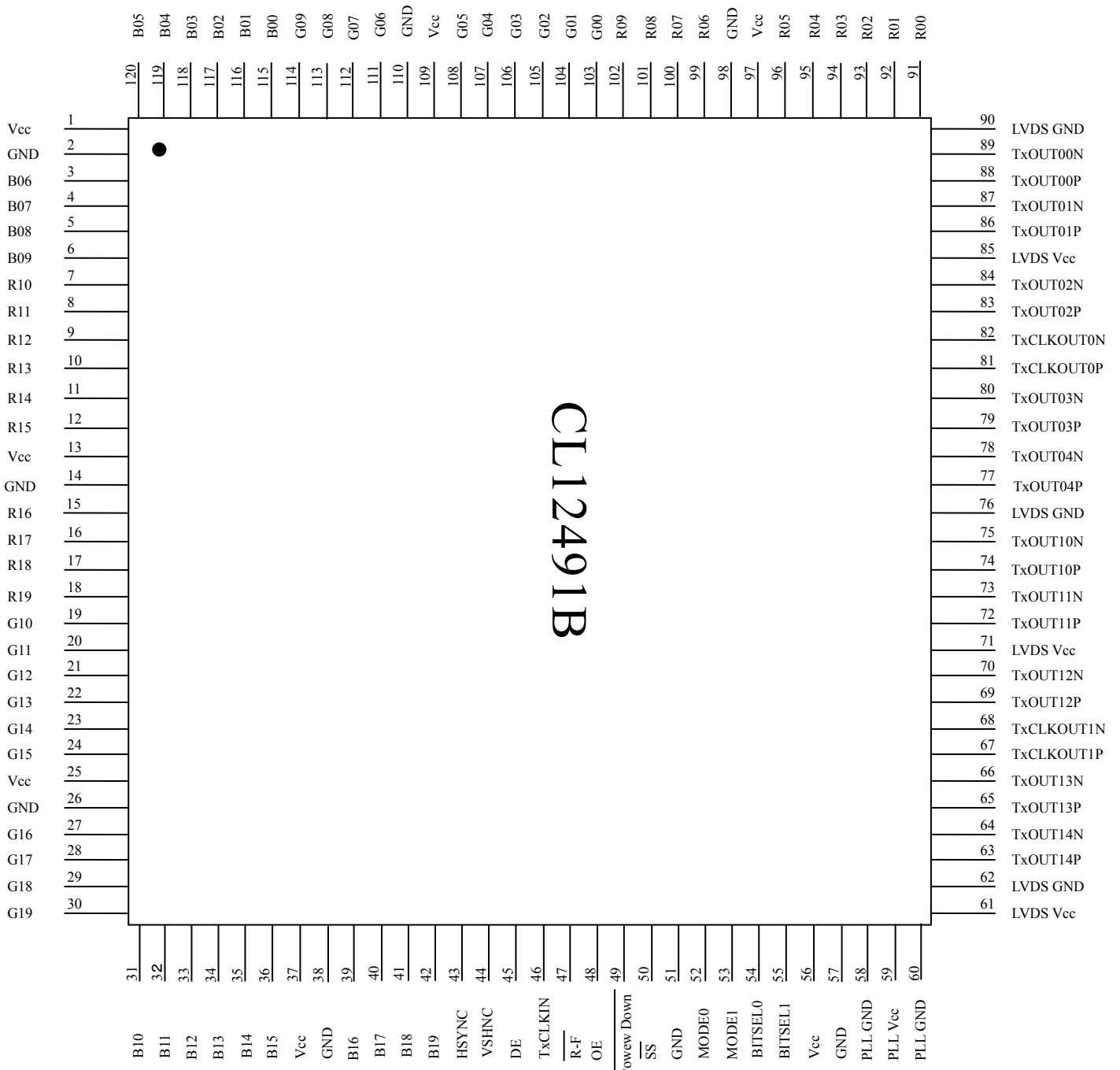
Feature

- 20MHz to 270MHz shift clock support
- Low power single 3.3V
- Clock edge programmable
- Supports VGA, SVGA, XGA, SXGA, UXGA, QXGA
- Supports Dual Link and Single Link
- Supports RGB 18 / 24 / 30
- Narrow bus reduces cable size
- PLL requires no external components
- Power down mode
- 345mV swing LVDS devices for low EMI
- Supports 200mV Differential Amplitude Outputs
- Low Profile 120 Lead TQFP Package

Block Diagram



Pin Configuration



Pin Description

Pin Name	No of Pin	I/O	Pin Description																		
TxOUT00N~04N	10	OUT	1st Link LVDS Differential Data Outputs																		
TxOUT00P~04P			The 1st pixel output data when Dual Link																		
TxCLKOUT0N/0P	2	OUT	1st Link LVDS Differential Clock Outputs																		
TxOUT10N~10N	10	OUT	2nd Link LVDS Differential Data Outputs																		
TxOUT10P~10P			These pins are disabled when Single Link																		
TxCLKOUT1N/1P	2	OUT	2nd Link LVDS Differential Clock Outputs																		
R00~R09	30	IN	1st Pixel LVCMOS Data Inputs																		
G00~G09																					
B00~B09																					
R10~R19	30	IN	2nd Pixel LVCMOS Data Inputs																		
G10~G19																					
B10~B19																					
TxCLKIN	1	IN	LVCMOS Level Clock Input																		
DE	1	IN	Data Enable Input																		
VSYNC	1	IN	Vsync Input																		
HSYNC	1	IN	Hsync Input																		
OE	1	IN	H: Output Enable L: Output Disable (All Outputs are Hi-Z)																		
<u>Power Down</u>	1	IN	H: Normal Operation L: Power Down (All Outputs are Hi-Z)																		
<u>R_F</u>	1	IN	Programmable Strobe Select H: Rising Edge, L: Falling Edge																		
SS	1	IN	Programmable Differential Amplitude Voltage Select H: 345mV, L: 200mV																		
MODE0/MODE1	2	IN	Data Mode <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>MODE</th> <th>MODE</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>L</td> <td>L</td> <td>Dual Link (Dual-in/Dual-out)</td> </tr> <tr> <td>L</td> <td>H</td> <td>Not use</td> </tr> <tr> <td>H</td> <td>L</td> <td>Not use</td> </tr> <tr> <td>H</td> <td>H</td> <td>Single Link (single-in/single-out)</td> </tr> </tbody> </table>	MODE	MODE	Mode	1	0		L	L	Dual Link (Dual-in/Dual-out)	L	H	Not use	H	L	Not use	H	H	Single Link (single-in/single-out)
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Vcc / GND	8/8	IN	Power Supply/Ground Pins for LVCMOS Inputs																		
PLL Vcc / PLL GND	1/2	IN	Power Supply/Ground Pins for PLL																		
LVDS Vcc / LVDS GND	3/3	IN	Power Supply/Ground Pin for LVDS Outputs																		