Introduction

The CL12501IP336 Transmitter converts 18bits LVCMOS parallel data of RGB into 3-channnel mini-LVDS serial data streams. A Phase-locked transmit clock is transmitter in parallel with the data streams. The CL12501IP336 transmitter is programmed for rising edge or falling edge clocks through a dedicated pin. At a transmit clock frequency of 336MHz, 18bits of RGB data are transmitted at a rate of 672Mbps per mini-LVDS data channel. The CL12501IP336 Transmitter is an ideal means to solve EMI and cable size problems associated with wide, high speed CMOS interface.

Feature

- Input Clock: 20MHz to 112MHz (max: 135MHz) shift clock support
- Output Clock: 60MHz~336MHz (max: 405MHz)
  Output Data Rate: 120Mbps~672Mbps (max: 810Mbps)
- Low power single 3.3V (Option: 2.5 / 2.8V) (Option: 1 / 1.2 / 1.5 / 1.8V Logic/Level Shifter)
- Clock Edge Programmable
- Supports VGA, SVGA, XGA, SXGA, SXGA+
- Narrow bus reduces cable size
- PLL requires no external components
- Power down mode
- ±200mV swing mini-LVDS for low EMI
- mini-LVDS format

Block Diagram