Introduction

The CL12512IP340 Receiver converts the 3-channnel mini-LVDS serial data streams back to parallel 24bits of LVCMOS (each other 8bit, total 24bits of RGB data). The CL12512IP340 Receiver is an ideal means to solve EMI and cable size problems associated with wide, high speed CMOS interface.

Feature

- Input Clock: 80MHz to 340MHz (max: 448MHz)
  Input Data Rate: 160Mbps~680Mbps (max: 896Mbps)
- Output Clock: 20MHz~85MHz (max: 112MHz) shift clock support
- Low power single 3.3V (Option: 2.5 / 2.8V) (Option: 1 / 1.2 / 1.5 / 1.8V Logic/Level Shifter)
- Supports VGA, SVGA, XGA, SXGA , SXGA+
- Narrow bus reduces cable size
- Power down mode
- mini-LVDS format

Block Diagram