

Introduction

The CL12623IP650 Transmitter converts LVCMOS parallel data (81.25MHz) of 8-bit into each other channel sub-LVDS serial clock/data (650Mbps) streams. This chipset is an ideal means to link mobile camera modules Baseband processors. A configurable input pin (CLS) is provided to select different Class (0 or 1, 2) mode inside the SMIA standard specifications. And DDR format mode support for mode pin (MDS). The CL12623IP650 Transmitter is an ideal means to solve EMI and cable size problems associated with wide, high speed CMOS interface.

Feature

- Input Clock: 20MHz~81.25MHz shift clock support
- Output Clock: 80MHz~325MHz Output Data rate: 160Mbps~650Mbps
- LVCMOS Input, sub-LVDS Output
- SMIA / CCP Class0, 1, 2 compliant
- CCP Class0, CCP Class1, 2 supports (CLS pin)
- DDR Format support (MDS pin)
- High Speed Rate
 - Parallel Input: ~81.25MHz (CLK0, 1, 2, D0, 1, 2<7:0>)
 - Serial Output: CCP Class0 ~208Mbps (Data0, 1, 2+/-, Clk0, 1, 2+/-)
 - CCP Class1, 2 208~650Mbps (Data0, 1, 2+/-, Strb0, 1, 2+/-)
 - DDR Format ~650Mbps (Data0, 1, 2+/-, Clk0, 1, 2+/-)
- 2.8~3.3V (Option: 1.2 / 1.8v) supply voltage (Option: 1.0 / 1.2 / 1.8v Logic/Level Shifter)
- Clock Edge Programmable (R_F pin)
- MSB/LSB Programmable (SBS pin)
- ±150mV swing sub-LVDS for low EMI
- Power Down Mode ~1μA (PD pin)

Block Diagram

