

Introduction

The CL12624IP650 Receiver convert sub-LVDS Clock/Data streams (~650Mbps) back into parallel 8-bits of LVC MOS. The output LVC MOS clock is transmitted in parallel with data. This chipset is an ideal means to link mobile camera modules Baseband processors. A configurable input pin (CLS) is provided to select different Class (0 or 1, 2) mode inside the SMIA standard specifications. And DDR format mode support for mode pin (MDS). The CL12624IP650 Transmitter is an ideal means to solve EMI and cable size problems associated with wide, high speed CMOS interface.

Feature

- Input Clock: 80MHz~325MHz Output Data Rate: 160Mbps~650Mbps
- Output Clock: 20MHz~81.25MHz shift clock support
- sub-LVDS input, LVC MOS output
- SMIA / CCP Class0, 1, 2 compliant
- CCP Class0, CCP Class1, 2 supports (CLS pin)
- DDR Format support (MDS pin)
- High Speed Rate
 - Serial Input: CCP Class0 ~208Mbps (Data0, 1, 2+/-, Clk0, 1, 2+/-)
 - CCP Class1,2 208~650Mbps (Data0, 1, 2+/-, Strb0, 1, 2+/-)
 - DDR Format ~208Mbps (Data0, 1, 2+/-, Clk0, 1, 2+/-)
- Parallel Output: ~81.25MHz (CLK0, 1, 2, D0, 1, 2<7:0>)
- 2.8~3.3V (Option: 1.8V) supply voltage (Option: 1.0 / 1.2 / 1.8V Logic/Level Shifter)
- Clock Edge Programmable (R_F pin)
- MSB/LSB Programmable (SBS pin)
- ±150mV swing sub-LVDS for low EMI
- Narrow bus reduces cable size
- Power Down Mode ~1μA (PD pin)
- Supports Fail-Safe function to all input channels

Block Diagram

