Introduction

The CL12633IP1000 is an ideal means to link mobile camera modules to baseband processers and baseband processers to LCD panels. The CL12633IP1000 is designed to support data rate in excess of 1Gbps utilizing MIPI-DPHY specification. The differential outputs provide low EMI with its typical low output swing of 200mV.

Feature

- Serial Clock Frequency 80MHz-500MHz (max: 1GHz)
  - Both Edge: Input Data Rate 160Mbps-1Gbps (max: 2Gbps)
  - Single Edge: Input Data Rate 80Mbps-500Mbps (max: 1Gbps)
- Parallel Clock Frequency 20MHz~125MHz (max: 250MHz)
- MIPI Alliance Specification for DPHY v1.00.00 compliant
- Low Power single 1.2V (Option: 1.5 / 1.8 / 2.8 / 3.3V)
- 200mV swing MIPI-DPHY for low EMI
- Maximum Port: Clock 1 port / Data 1-4 port
- PLL / Escape Mode / Fail-safe circuit Options (Not include Lane control circuit)

Block Diagram