

**Introduction**

The CL12671IP Multi-Transmitter converts LVCMOS parallel data of 8-bit into each other channel MIPI –DPHY and MDDI ver.1.2 serial clock (strobe)/data streams. This chipset is an ideal means to link mobile camera modules Baseband processors. And MIPI-DPHY and MDDI format mode support for mode pin (MDS). The CL12671IP Transmitter is an ideal means to solve EMI and cable size problems associated with wide, high speed CMOS interface.

**Feature**

- Input Clock: 20MHz~125MHz shift clock support
- Output Clock: 80MHz~500MHz, Output Data rate: 160Mbps~1Gbps
- LVCMOS Input, Differential Output
- MIPI-DPHY Ver.1.00.00 / MDDI ver.1.2 compliant
- MIPI-DPHY / MDDI ver.1.2 Format support (MDS pin)
- High Speed Rate
 

Parallel Input:		~125MHz (CLKI0~ n, DI0~n<7:0>)
Serial Output:	MIPI-DPHY	~1Gbps (Data0~n+/-, Clk+/-)
	MDDI ver.1.2	~1Gbps (Data0~n+/-, Clk+/-)
- 1.8V (Option: 2.8/3.3v) supply voltage (Option: 1.0 / 1.2 / 1.8v Logic/Level Shifter)
- Clock Edge Programmable (R\_F pin)
- MSB/LSB Programmable (SBS pin)
- ±150/200mV swing differential signal for low EMI
- Power Down Mode ~1μA (PD pin)

**Block Diagram**

