Introduction

The CL12684MR3AM6AIC is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to Host System. The CL12684M4R3AM6AIC is designed to support data rate in excess of maximum 1Gbps utilizing sub-LVDS / mini-LVDS / LVDS / HiSPi(SLVS-400, HiVCM) / MIPI-DPHY / CMOS interface specification. The CL12684M4R3AM6AIC can change Interface type to same PAD for changing mode.

Feature

- MIPI DPHY v1-1 / MIPI CSI / TIA/EIA-644 LVDS / SLVS-400 compliant
- Differential signal of almost CIS serial and parallel inputs support
  1) sub-LVDS Serial / Parallel
  2) mini-LVDS (Reduce Mode LVDS) * SLVS-200
  3) LVDS
  4) HiSPi (SLVS-400, HiVCM)
  5) MIPI DPHY
  6) CMOS 1.8V
- LVDS 2bit serial outputs support for LVOMODE pin
- Differential inputs to LVDS outputs support for LVOMODE and TSTADOxx pin
- Maximum Input Clock Frequency: ~500MHz Maximum Input Data Rate: ~1Gbps
- Maximum Output Clock Frequency: ~500MHz Maximum Output Data Rate: ~500Mbps
- Power Voltage: Analog 1.8V / Digital 1.8V
- Maximum Serial Input Ports(Lanes): Clock 1-port / Data 4-ports (lanes)
- Output Serial Clock Edge Programmable for FRPCK pin
- Output Format 2/4/8bit Selectable for BTSEL[1:0]
- MSB/LSB Selectable for SBSEL pin
- Using for receiver of almost CMOS Image Sensor (Panasonic/Sony/Aptina/OVT/AltaSels/ST-micro e.t.c.)
- Power Consumption: (Process: FF, Temperature: 125, Power Voltage: max) $I_{TOTAL}=V_{CC}+V_{DD}$
  - Active maximum 100mA
  - Sleep maximum 10uA (for PWDN pin)
- ESD (HBM / MM / CDM / Latch Up): 2kV / 200V / 500V / 100mA

Package and Pin Assignment

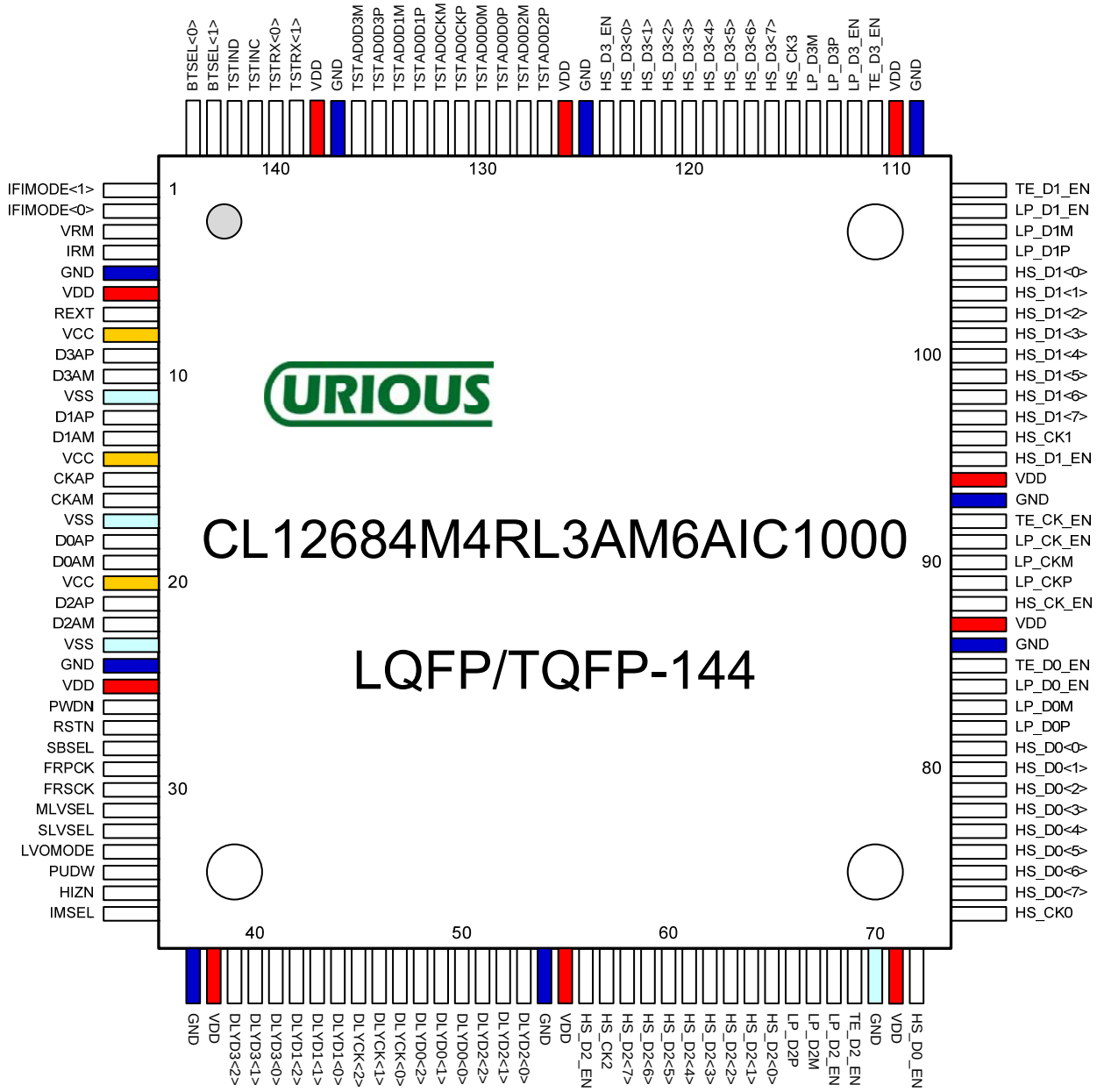

Fig.1-1 LQFP-144 Package and Pin Assignment

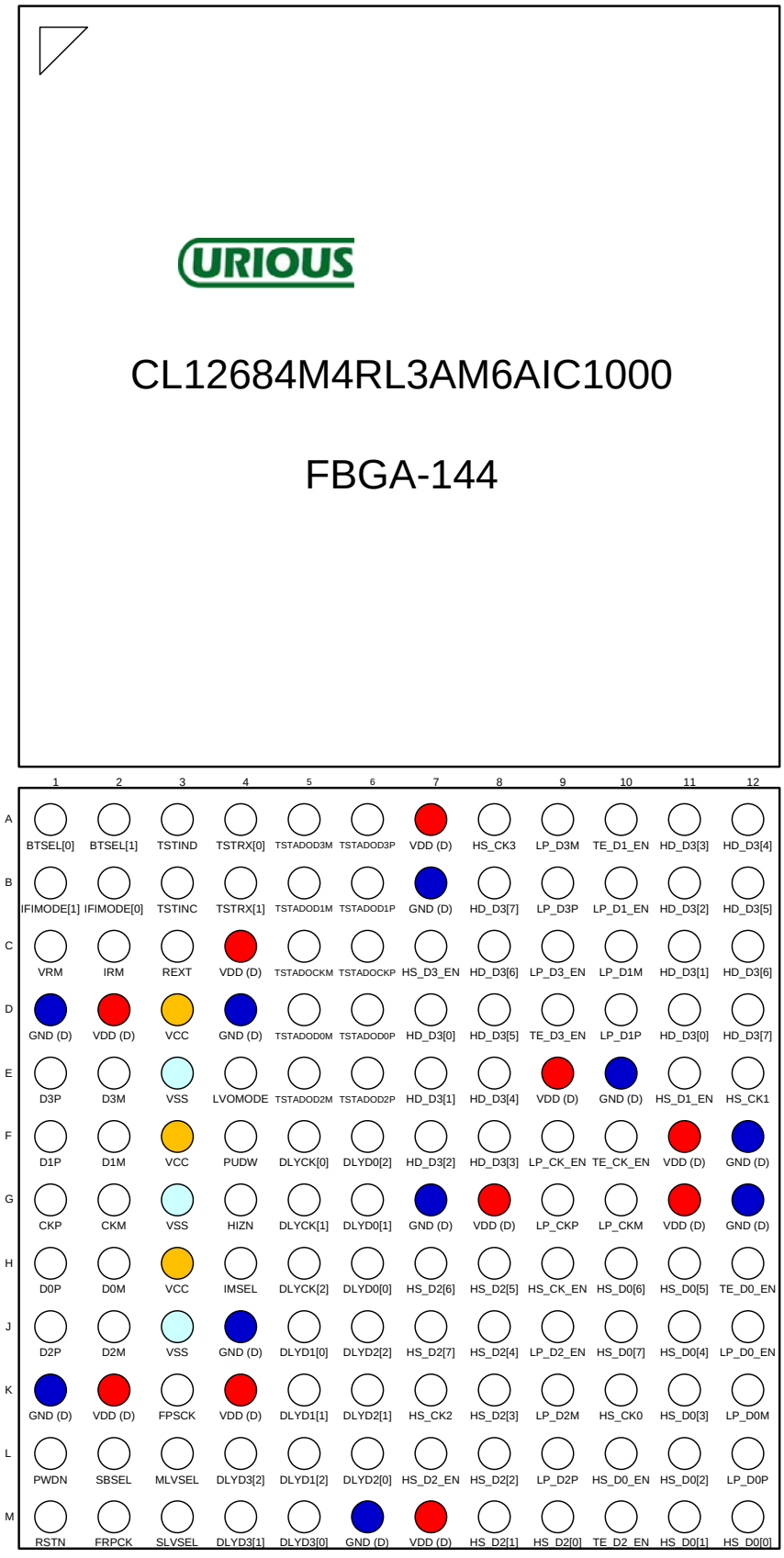

Fig.1-2 FBGA-144 Package and Pin Assignment