Introduction

The CD12683IP is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to Host System. The CD12683IP is designed to support MIPI D-PHY/sub-LVDS(LVDS)/HiSPi(SLVS-400)/CMOS serial interface bitmap. The CD12683IP is supported RAW 10/12/14bit outputs.

Feature

- MIPI CSI-2
  - Support Pixel to byte packing: RAW8, 10, 12, 14 (Optional: YUV, RGB, JPEG)
  - Support Lane management: 1, 2, 4 Lane (Optional: 6, 8, 12, 16 Lane)
  - Support Low Level Protocol
    - -- Short Packet Format, Long Packet Format
    - -- ECC and Check Sum
    - -- (Optional: Virtual Channel Identifier)
    - -- (Optional: Embedded Information)
- sub-LVDS (LVDS)/HiSPi(SLVS-400)/CMOS custom link
  - Support Pixel to byte packing: RAW8, 10, 12, 14 (Optional: Custom Data Packing)
  - Support Lane management: 1, 2, 4 Lane (Optional: 6, 8, 12, 16 Lane)
  - Support Protocol: Generic Sync Code Format
    *Register Parameter Configuration
    (Optional: Custom Code & Operation)
- Link User System and Total System Design
  - Total Trans Rate Design
    - -- Operation Frequency
    - -- Optimization Circuit Scale
  - (Optional: Memory Interface)
    - -- (Optional: Parallel Pixel I/F)
    - -- (Optional: Bus System (AMBA/AXI/etc...))
  - (Optional: Sync Signal Generator)
- Using for receiver of MIPI D-PHY/sub-LVDS (LVDS)/HiSPi(SLVS-400)/CMOS CIS (Sony/Panasonic/OmniVision/Aptina/Toshiba/etc...)

Block Diagram