Introduction

The CD12702IP is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to Host System. The CD12702IP is designed to support HiSPi (SLVS-400) serial interface bitmap. The CD12702IP is supported RAW 10/12/14bit outputs.

Feature

- HiSPi (SLVS-400) custom link
  - Support Pixel to byte packing: RAW8, 10, 12, 14 (Optional: Custom Data Packing)
  - Support Lane management: 1, 2, 4 Lane (Optional: 6, 8, 12, 16 Lane)
  - Support Protocol: Generic Sync Code Format
    *Register Parameter Configuration
    (Optional: Custom Code & Operation)
- Link User System and Total System Design
  - Total Trans Rate Design
    -- Operation Frequency
    -- Optimization Circuit Scale
  - (Optional: Memory Interface)
    -- (Optional: Parallel Pixel I/F)
    -- (Optional: Bus System (AMBA/AXI/etc...))
  - (Optional: Sync Signal Generator)
- Using for receiver of HiSPi (SLVS-400) CMOS Image Sensor (Aptina/etc...)

Block Diagram