Introduction

The CL12684K/M4/12/16R3AM6/7AIP is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to Host System. The CL12684K/M4/12/16R3AM6/7AIP is designed to support data rate in excess of maximum 1Gbps utilizing sub-LVDS / mini-LVDS / LVDS / HiSPi(SLVS-400, HiVCM) / MIPI-DPHY / CMOS-1.8V / CMOS-3.3V interface specification. The CL12684K/M4/12/16R3AM6/7AIP can change Interface type to same PAD for changing mode.

Feature

- MIPI DPHY v1-1 / MIPI CSI / TIA/EIA-644 LVDS / SLVS-400 compliant
- Differential signal of almost CIS serial inputs support
  1) sub-LVDS Serial / Parallel
  2) mini-LVDS (Reduce Mode LVDS)
  3) LVDS
  4) HiSPi (SLVS-400, HiVCM)
  5) MIPI DPHY
  6) CMOS 1.8V
  7) CMOS 3.3V (CL12684M4/12/16R3AM7AIP Only)
- Maximum Input Clock Frequency: ~500M/750MHz Maximum Input Data Rate: ~1G/1.5Gbps
- Maximum Output Clock Frequency: ~500M/750MHz Maximum Output Data Rate: ~500M/750Mbps
- Power Voltage:
  -CL12684K4/12/16R3AM6AIP: Analog 2.5V / Digital 1.0V (T55GP)
  -CL12684M4/12/16R3AM6/7AIP: Analog 1.8V / Digital 1.1V (T40LP/S40LL)
  -CL12684M4/12/16R3AM6/7AIP: Analog 1.8V / Digital 0.9V (T28HPC)
- Maximum Serial Input Ports(Lanes):
  -CL12684K/M4R3AM6/7AIP: Clock 1-port / Data 4-ports (lanes) x1
  -CL12684K/M12R3AM6/7AIP: Clock 1-port / Data 4-ports (lanes) x3
  -CL12684K/M16R3AM6/7AIP: Clock 1-port / Data 4-ports (lanes) x4
- Parallel Input 12/14/16bit support for CKIMODE pin (Using CKB only mode)
  -CL12684K/M4R3AM6/7AIP: Parallel 12/14/16bit support for using 3-IP or 4-IP
  -CL12684K/M12R3AM6/7AIP: Parallel 12bit support
  -CL12684K/M16R3AM6/7AIP: Parallel 12/14/16bit support
- Output Serial Clock Edge Programmable for FRPCK pin
- Output Format 2/4/8bit Selectable for BTSEL[1:0]
- MSB/LSB Selectable for SBSEL pin
- Using for receiver of almost CMOS Image Sensor (Panasonic/Sony/Aptina/OVT/AltaSels/ST-micro e.t.c.)
- Power Consumption: (Process: FF, Temperature: 125, Power Voltage: max) $I_{TOTAL}=V_{CC}+V_{DD}$
  - Active maximum
    -CL12684K/M4R3AM6/7AIP: 14.8mA
    -CL12684K/M12R3AM6/7AIP: 42.4mA
    -CL12684K/M16R3AM6/7AIP: 56.2mA
  - Sleep maximum 10uA (for PWDN pin)
- Layout Size: (Before Shrink)
  -CL12684K4/12/16R3AM6AIPT055GP: 575/1275/1695 x 567.5 um (35 um PAD pitch. Not I/O Cell)
  -CL12684M4/12/16R3AM7AIPS040LL: 540/1140/1500 x 435.0 um (30 um PAD pitch, Not I/O Cell)
  -CL12684M4/12/16R3AM6AIPT040LP: 540/1140/1500 x 435.0 um (30 um PAD pitch, Not I/O Cell)
  -CL12684M4/12/16R3AM7AIPT028HPC:540/1140/1500 x 860.0 um (30 um PAD pitch, Not I/O Cell)
- Process:
  -CL12684K4/12/16R3AM6AIPT055GP: TSMC 55nm Generic Process 1P7M (5x1Z)
  -CL12684M4/12/16R3AM6AIPS040LL: SMIC 40nm Low Leak 1P8M (6M+2TM)
  -CL12684M4/12/16R3AM6AIPT040LP: TSMC 40nm Low Power 1P8M (6M+2TM)
  -CL12684M4/12/16R3AM7AIPT028HPC: TSMC 28nm High Performance Compact 1P8M (6M+2TM)
- ESD (HBM / MM / CDM / Latch Up): 2kV / 200V / 500V / 100mA

■ Verified Operation CMOS Image Sensor for customers (November/2013)

- **Panasonic** MN34220, MN34210, MN34041, MN34031
- **Sony** IMX136
- **OmniVision** OV10810, OV10633, OV14825, OV4688, OV3630 OV2715, OV2710
- **Aptina** MT9P006, AR0331
- **Micron(Aptina)** MI5100(MT9P001), MI1320(MT9D112)
- **CMOSIS** CMV2000

■ Delivery Item:

1) Standard
- Verilog Model (verilog / vcs)
- .db file
- symbol
- LVS netlist
- LEF file
- layer map file
- layout technology file
- layout Verification Report (DRC & LVS)
- layout Verification Command file
- Datasheet (This file)
- Application Note (Usage connection CIS, e.t.c.)
- Packaging and Layout Guideline
- PCB Guideline
- STA (Static Delay Analysis) Guideline

2) Options
- .lib file (Option)
- Hspice netlist for using board simulation (Option)
- IBIS Model (Option)
- Testing Guideline (Option)
- CL12683M4T3AM6AIC 6-mode multiple (Combo)-Transmitter IC BOST (Option)
- CL12683M4T3AM6AIC 6-mode multiple (Combo)-Transmitter Board BOST (Option)
- CL12683M4T3AM6AIC 6-mode multiple (Combo)-Transmitter Datasheet BOST (Option)
- CL12683M4T3AM6AIC 6-mode multiple (Combo)-Transmitter Verilog Model BOST (Option)
- CL12683M4T3AM6AIC 6-mode multiple (Combo)-Transmitter Verilog Test Vector BOST (Option)
- CMOS Sensor Verilog Model (Panasonic, Sony, Aptina, MIPI, etc) (Option)
- Receiver single or multiple Link-Layer (Output RAW10/12bit, YUV, RGB, etc) (Option)
- Image Signal Processing (ISP) IP (Option)
- FPGA Board (Including CL12684M4R3AM6AIC Receiver IC) (Option) T.B.D.
- CL12684M4R3AM6AIC 6-mode multiple (Combo)-Receiver IC (Option)