Introduction

The CL12822M8LRM2AM2DIP2500 is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to ISP (Imaging Signal Processer) and DSP. The CL12822M8LRM2AM2DIP2500 is designed to support data rate in excess of maximum 2.5Gbps utilizing SLVS-EC / MIPI-DPHY interface specification. The CL12822M8LRM2AM2DIP2500 can change Interface type to same PAD for changing mode.

Feature

- SLVS-EC ver.1.2 / MIPI D-PHY ver.1-1 compliant
- Supporting for two kind Differential Input Signals
  - 1) SLVS-EC (Maximum 2.5Gbps)
  - 2) D-PHY (Maximum 1.5Gbps) High Speed Only
  - 3) CMOS 1.8V (Maximum 100MHz)
- Xtal Input Clock Frequency Selectable 24MHz / 72MHz
- Maximum Input Clock Frequency ~1.25GHz, Maximum Input Data Transfer Rate ~2.5Gbps
- Maximum Output Clock Frequency ~250MHz
- Power Supply : Vcc=1.8V (IO and Analog) Vdd=1.1V (Inside Core)
- Lane Number : 8-Lane
- 10-bit / Lane Parallel Outputs(SLVS-EC), 8-bit / Lane Parallel Outputs(D-PHY)
- Including Power Down Mode
- Including Z-Impedance Detect Circuit
- Consumption Current (Condition Process: FF, Temperature: -40-degree, Supply Voltage: Maximum)
  - Maximum Operation Current: Total: 132mA (Vcc: 86.2mA, Vdd: 45.8mA)
  - Maximum Power Down Current: 10uA
- Layout Size:
  - （Including ESD IO Cell and 2nd ESD Cell）
    - 1460.225 um × 2400.00 um (Before Shrink)
    - 1314.200 um × 2160.00 um (After Shrink)
  - （Not Including ESD IO Cell and 2nd ESD Cell）
    - 1460.225 um × 2157.88 um (Before Shrink)
    - 1314.200 um × 1942.09 um (After Shrink)
- UMC 40nm LP Process (Using of Standard Vth Transistor)
- Supporting Link-layer for CD12822S8LRM2AIP2500 (SLVS-EC link and CSI2 Combo) soft macro