Introduction

The CL12842M4LRM2AM2DIC2304 is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to ISP (Imaging Signal Processer) and DSP. The CL12842M4LRM2AM2DIC2304 is designed to support data rate in excess of maximum 2.304Gbps utilizing SLVS-EC / sub-LVDS / MIPI D-PHY / CMOS 1.8V interface specification. The CL12842M4LRM3AM4AIC2304 can change Interface type to same PAD for changing mode.

Feature

- SLVS-EC ver.1.2 / MIPI D-PHY ver.1-1 compliant
- Supporting for two kind Differential Input Signals
  1) SLVS-EC (Maximum 2.304Gbps)
  2) sub-LVDS (Maximum 650Mbps)
  3) MIPI D-PHY (Maximum 1.5Gbps)
  4) CMOS 1.8V (Maximum 150MHz)
- Xtal Input Clock Frequency Selectable 24MHz / 72MHz
- Maximum Input Clock Frequency ~1.152GHz, Maximum Input Data Transfer Rate ~2.304Gbps
- Maximum Output Clock Frequency ~115.2MHz(LVCMOS)/230.4MHz(LVDS)
- Power Supply : Vcc=1.8V (IO and Analog) Vdd=0.9V (Inside Core)
- Maximum Lane Number : 4-Lane
- 10-bit/Lane Parallel Outputs (SLVS-EC)
  8-bit/Lane Parallel Outputs (sub-LVDS Serial / MIPI D-PHY)
  1-bit/Lane Parallel Outputs (sub-LVDS Parallel)
- Including Power Down Mode
- Including "Hi-Z" Detect Circuit for SLVS-EC
- Supporting Link-layer for CD12842S12LRM3AIP2304 (SLVS-EC/LVDS, CSI2 Combo) soft macro

Package and Pin Assignment

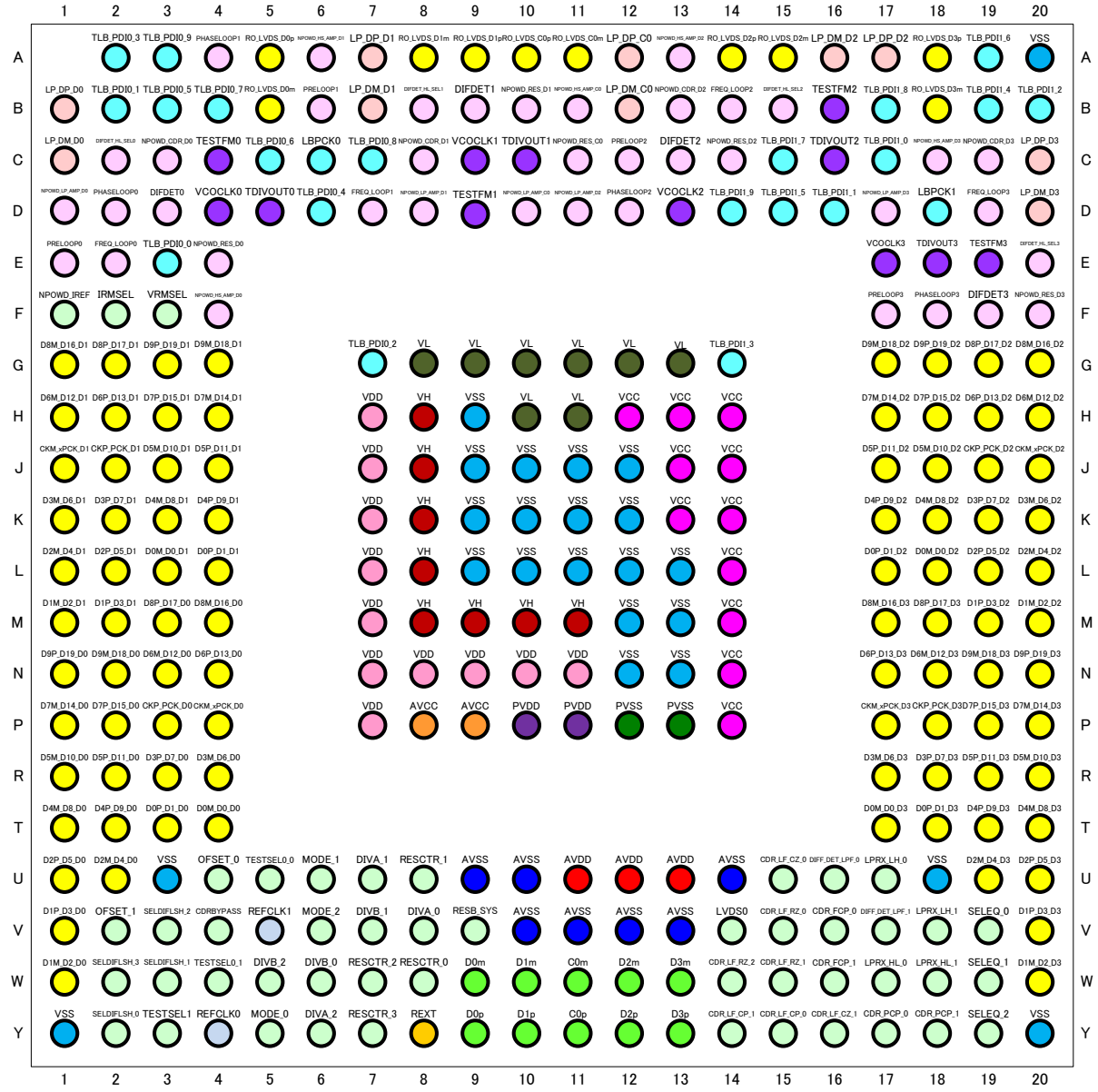

Fig.1-1 LFBGA Package Pin Assignment