Introduction

The CL12632M4R1AS1BIP4500 is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to ISP (Imaging Signal Processer) and DSP. The CL12632M4R1AS1BIP4500 is designed to support data rate in excess of maximum 4.5Gbps utilizing MIPI D-PHY v2-0 interface specification.

Feature

- MIPI D-PHY v2-0 / MIPI CSI2 compliant
- Supporting for four kind Differential Input Signals: MIPI D-PHY (Maximum 4.5Gbps)
- Maximum Input Clock Frequency: ~2.25GHz ,
- Maximum Input Data Transfer Rate: ~4.5Gbps
- Power Supply : Vcc=1.8V (IO and Analog) Vdd=0.9 V (Inside Core)
- Maximum Lane Number : 4-Lane
- 8-bit/Lane Parallel Outputs
- Including Power Down Mode
- TSMC 28nm HPC+
- Poly Direction: South-North
- Various process porting support available (Please contact us.)
- Supporting Link-layer: CD12632IP soft macro

If you have any questions or requirements,
such as a detailed information of Curious IP products,
please feel fee to contact us at the email address :
curious.info@curious-jp.com