Introduction

The CL12661K4T1AM2JIP is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to Host System. The CL12661K4T1AM2JIP is designed to support data rate in excess of maximum 1.5Gbps utilizing sub-LVDS / MIPI-DPHY interface specification. The CL12661K4T1AM2JIP can change Interface type to same PAD for changing mode.

Feature

- MIPI DPHY v1-1 / MIPI CSI2 compliant
- Differential signal of almost CIS serial outputs support
  1) sub-LVDS (Maximum 1.0Gbps)
  2) MIPI-DPHY (Maximum 1.5Gbps)
- Input Clock Frequency:
  (sub-LVDS mode Clock Generator Input) SCK=~1000MHz
  (MIPI-DPHY mode Clock Generator Input) SCK=~1500MHz
  (sub-LVDS 8/10/12/14/16 bit SER) PCK_N= ~100MHz
  (MIPI-DPHY 8bit SER) PCK_N= ~313MHz
- Output Clock Frequency: ~750MHz Output Data Rate: ~1.5Gbps
- Power Supply : 1.8V(I/O, Analog) 1.1V(Core)
- Max TX Lane Number: Clock 1-port / Data 4 -ports (lanes)
- Data Input Path:
  1) MIPI DPHY (8bit Parallel)
  2) Others (8, 10, 12, 14, 16 bit Parallel)
- Include Power Down Mode
- Output impedance Adjustable in settings
- Process TSMC 40LP
- Various process porting support available (Please contact us.)
- Supporting Link-layer (Soft Macro): CD12661IP

If you have any questions or requirements,
such as a detailed information of Curious IP products,
please feel fee to contact us at the email address :
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