Introduction

The CL12661M8T1KM2JIP is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to Host System. The CL12661M8T1KM2JIP is designed to support data rate in excess of maximum 2.5Gbps utilizing sub-LVDS / MIPI-DPHY interface specification. The CL12661M8T1KM2JIP can change Interface type to same PAD for changing mode.

Feature

- MIPI DPHY v1-2 / MIPI CSI2 compliant
- Differential signal of almost CIS serial outputs support
  1) sub-LVDS (Maximum 800Mbps)
  2) MIPI-DPHY (Maximum 2.5Gbps)

- Xtal Input Clock Frequency Selectable: 24 - 72MHz
- Input Clock Frequency:
  (sub-LVDS 8/10/12/14/16 bit SER) PCK_N= ~100MHz
  (MIPI-DPHY 8bit SER) PCK_N= ~313MHz
- Output Clock Frequency: ~1250MHz Output Data Rate: ~2.5Gbps
- Power Supply : 1.8V(I/O, Analog) 1.2V(LP_DRIVER) 0.9V(Core)
- Max TX Lane Number:
  sub-LVDS Clock 1-port / Data 8/4 -ports (lanes)
  MIPI-DPHY Clock 1-port / Data 4/2 -ports (lanes)
- Data Input Path:
  1) MIPI DPHY (8bit Parallel)
  2) Others (8, 10, 12, 14, 16 bit Parallel)
- Include Power Down Mode
- Output impedance : Adjustable in settings
- Process TSMC 28HPC+ (1P10M_5X2Y2R) Regular Vth only
- Various process porting support available (Please contact us.)
- Supporting Link-layer (Soft Macro): CD12661IP

If you have any questions or requirements,
such as a detailed information of Curious IP products,
please feel fee to contact us at the email address :
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