Introduction

The CL12662K4R1AM2JIP1500 is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to ISP (Imaging Signal Processer) and DSP. The CL12662K4R1AM2JIP1500 is designed to support data rate in excess of maximum 1.5Gbps utilizing sub-LVDS / MIPI D-PHY v1-1 interface specification. The CL12662K4R1AM2JIP1500 can change Interface type to same PAD for changing mode.

Feature

- MIPI D-PHY v1-1 / MIPI CSI2 compliant
- Supporting for four kind Differential Input Signals:
  1) sub-LVDS (Maximum 1.0Gbps)
  2) MIPI D-PHY (Maximum 1.5Gbps)
- Maximum Input Clock Frequency: ~750MHz, Maximum Input Data Transfer Rate ~1.5Gbps
- Maximum Output Clock Frequency: ~187.5MHz
- Power Supply : Vcc=1.8V (IO and Analog) Vdd=1.1 V (Inside Core)
- Maximum Lane Number : 4-Lane
- Parallel Outputs: 8/10/12/14/16bit support
- Including Power Down Mode
- TSMC 40LP Process
- Various process porting support available (Please contact us.)
- Supporting Link-layer: CD12662IP soft macro

If you have any questions or requirements,
such as a detailed information of Curious IP products,
please feel fee to contact us at the email address :
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