Introduction

The CL12821I4T2JM2NIP2500 is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to Host System.
The CL12821I4T2JM2NIP2500 converts the input parallel data to the serial data and output it.
The CL12821I4T2JM2NIP2500 is designed to support maximum 2.5Gbps data rate utilizing SLVS-MI or mipi-DPHY_specification_v1-2

Feature

- SLVS-MI / MIPI-DPHY v1-2 compliant
- Supporting for two kind Differential Output Signals
  1) SLVS-MI (Maximum 2.5Gbps)
  2) MIPI-DPHY (Maximum 2.5Gbps)
- Input Clock Frequency:
  (SLVS-MI 10bit SER) PCK_N= ~250MHz
  (MIPI-DPHY 8bit SER) PCK_N= ~313MHz
- Output Clock Frequency: ~1250MHz Output Data Rate: ~2.5Gbps
- Power Supply : 2.8V, 1.2V(PLL/BGR) 1.2V(PHY)
- Max TX Lane Number: 4-Lane Clock 1-port / Data 4-ports
- Data Input Path:
  1) SLVS-MI (10bit Parallel)
  2) MIPI DPHY (8bit Parallel)
- Include Power Down Mode
- Include Output clock's On/Off Mode
- Include Dp, Dm polarity Control
- TPSCo 65nm BSB Process
  Triple well structure Layer: 7M/1L (1M～ 6 M, 9M, L) 1.2V / 3.3V Transistor
- Various process porting support available (Please contact us.)
- Supporting Link-layer (Soft Macro): CD12821

If you have any questions or requirements,
such as a detailed information of Curious IP products,
please feel fee to contact us at the email address :
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