Introduction

The CL12822M4R2JM2LIP5000 is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to ISP (Imaging Signal Processer) and DSP. The CL12822M4R2JM2LIP5000 is designed to support data rate in excess of maximum 5.0Gbps utilizing SLVS-EC ver.2.0 / MIPI D-PHY v2-1 interface specification. The CL12822M4R2JM2LIP5000 can change Interface type to same PAD for changing mode.

Feature

- SLVS-EC ver.2.0 / MIPI D-PHY v2-1 compliant
- Supporting for four kind Differential Input Signals
  1) SLVS-EC (Maximum 5.0Gbps)
  2) MIPI D-PHY (Maximum 4.5Gbps)
- Xtal Input Clock Frequency Selectable 24MHz / 48MHz / 72MHz
- Maximum Input Clock Frequency ~2.25GHz (D-PHY mode)
- Power Supply : Vcc=1.8V (IO and Analog) Vdd=0.9 V (Inside Core)
- Maximum Lane Number : 4-Lane
- 10-bit/Lane Parallel Outputs (SLVS-EC)
  8-bit/Lane Parallel Outputs (MIPI D-PHY)
- Including Power Down Mode
- Including "Hi-Z" Detect Circuit for SLVS-EC
- TSMC 28nm HPC+
- Poly Direction: South-North
- Various process porting support available (Please contact us.)
- Supporting Link-layer: CD12822IP soft macro

If you have any questions or requirements,
such as a detailed information of Curious IP products,
please feel fee to contact us at the email address :
curious.info@curious-jp.com