Introduction

The CL12832M8R2JM3QIP2500 is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to ISP (Imaging Signal Processer) and DSP. The CL12832M8R2JM3QIP2500 is designed to support data rate in excess of maximum 2.5Gbps utilizing SLVS-EC / MIPI D-PHY v-1.2/ CMOS 1.8V interface specification. The CL12832M8R2JM3QIP2500 can change Interface type to same PAD for changing mode.

Feature

- SLVS-EC ver.1.2 / MIPI D-PHY ver.1-2 compliant
- Supporting for four kind Differential Input Signals
  1) SLVS-EC (Maximum 2.4Gbps)
  2) MIPI D-PHY (Maximum 2.5Gbps)
  3) CMOS 1.8V (Maximum 166MHz)
- Xtal Input Clock Frequency Selectable 24MHz / 37.125MHz / 54MHz / 72MHz
- Maximum Input Clock Frequency ~1.25GHz, Maximum Input Data Transfer Rate ~2.5Gbps
- Maximum Output Clock Frequency ~312.5MHz
- Power Supply : Vcc=1.8V (IO and Analog) Vdd=0.9 V (Inside Core)
- Maximum Lane Number : 8-Lane
- 10-bit/Lane Parallel Outputs (SLVS-EC)
  8-bit/Lane Parallel Outputs (MIPI D-PHY)
- Including Power Down Mode
- Including "Hi-Z" Detect Circuit for SLVS-EC
- TSMC 28nm HPC Process 1P10M5X2R (Using of Standard Vth Transistor)
- Poly Direction: South-North
- Various process porting support available (Please contact us.)
- Supporting Link-layer: CD12832IP soft macro

If you have any questions or requirements,
such as a detailed information of Curious IP products,
please feel fee to contact us at the email address :
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