OVERVIEW

The CL12911IP4000 is based on MIPI A-PHY interface specification announced in year 2020, targeting ultra-high-speed networking applications in ADAS and autonomous drive subsystems. It supports applications that require long reach (up to 15 meters), error-free links, and high EMI immunity requirement.

PHY IP supports the SOURCE function of MIPI A-PHY Gear-2 stated in standard specification. It supports data rate up to 4Gbps with integrated mixed signal circuit, high performance TX driver, embedded TX clock generation, on chip optional termination resistor calibration.

This CL12911IP4000 A-PHY Source IP enables designers with the low area and low power with support for the leading process technologies in TSMC 40nmLP and Global Foundry 40nmLP process.

FEATURES

- Compliant with MIPI A-PHY specification version 1.0
- Support Gear-2 up to 4Gbps
- Support data bus width: 20-bit parallel interface
- Support 1 lane
- Support Uplink Receiver @ 100Mbps
- Selectable input clock frequency: 24MHz/72MHz
- Maximum output clock frequency at 200MHz
- Supports Single-ended coaxial or shielded twisted-pair (STP) cable up to 15m
- support A-PHY PMD layer by HARD macro
- AEC-Q100 (Grade 1) qualified for automotive applications
- High performance Data and clock recovery.
- Analog monitor port for test and debug
- Embedded termination Resistor and optional calibration function
- Supporting Link IP CD12911IP200 (PHY layer PCS, RTS and Data Link) soft macro
  Native Protocol Adaption layer supports (Option)

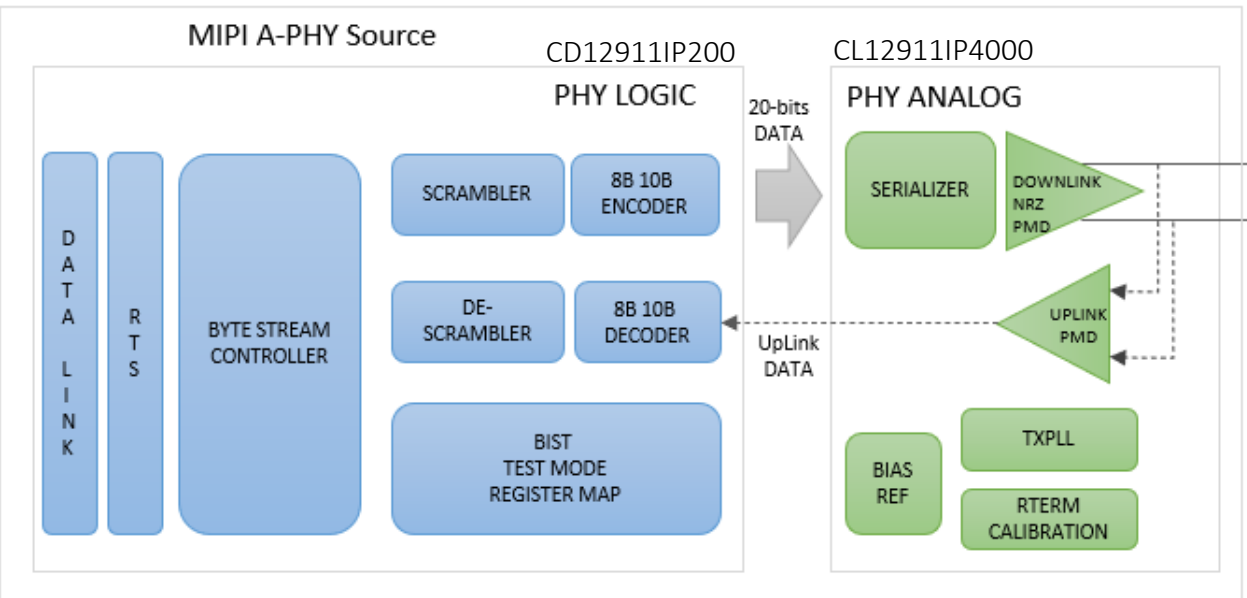

Figure 1 Generic block diagram of CL12911IP4000 and CD12911IP200

Parameters		Specification
Technology Node		TSMC40LP, GF 40nm LP
Compliance / Standard		MIPI A-PHY V1.0
Input Reference Clock		24MHz / 72MHz
Data Rate		≤ 4 Gbps
Number of Pad Required		TBD
Operating Condition	VDD11	1.00V ~ 1.20V
	VDD18	1.62V ~ 1.98V
	Temperature	-40C ~ 125C
IP Size		TBD

DELIVERABLES

- GDSII
- Place-Route views (.LEF)
- Liberty library (.lib)
- Verilog behavior model
- Netlist & Timing information
- Layout guidelines, application notes
- LVS/DRC verification reports

CURIOUS is a leading fabless design house specializing in high speed interface IP and mixed signal module for Image Sensors, Display and Data application.

For more information about CURIOUS IP, visit http://www.curious-jp.com

If you have any questions or requirements, such as a detailed information of Curious IP products, please feel free to contact us at the email address : curious.info@curious-jp.com